

# SMT-based task- and network-level static schedule generation for time-triggered networked systems

#### Silviu S. Craciunas, Ramon Serna Oliver

TTTech Computertechnik AG RTNS 2014, Versailles, France, October 5-8, 2014





#### Time Triggered Networks



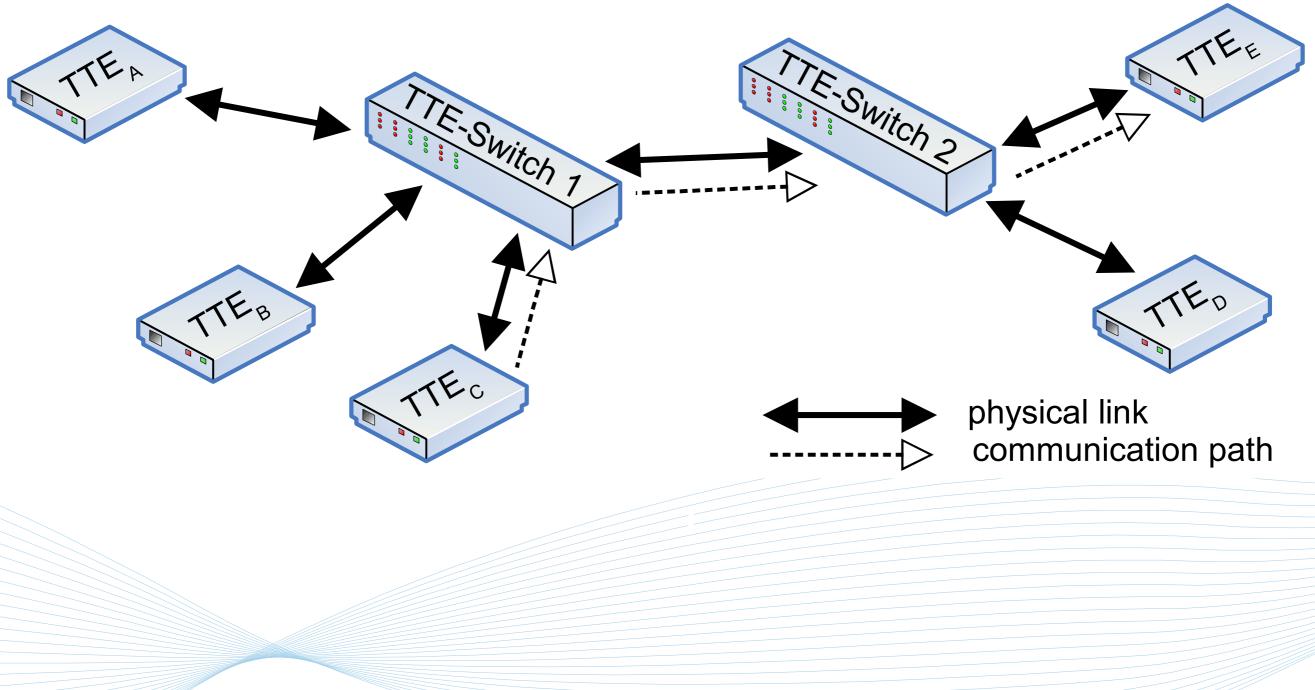


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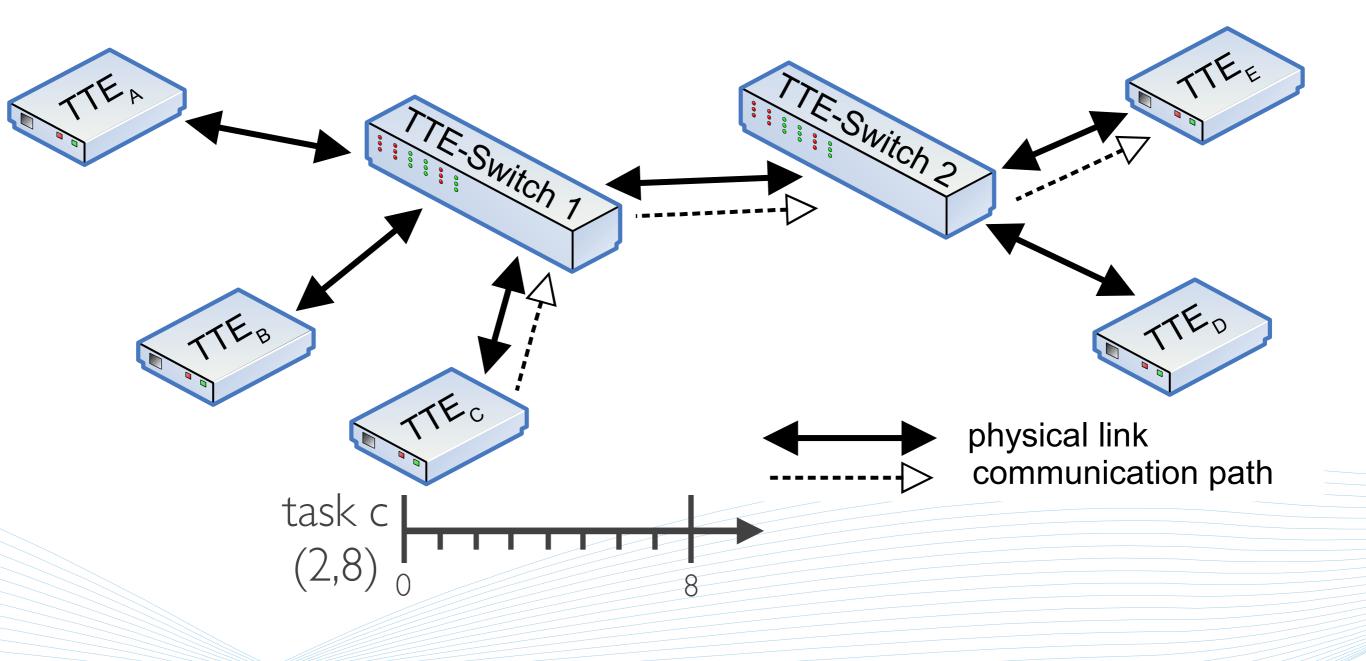




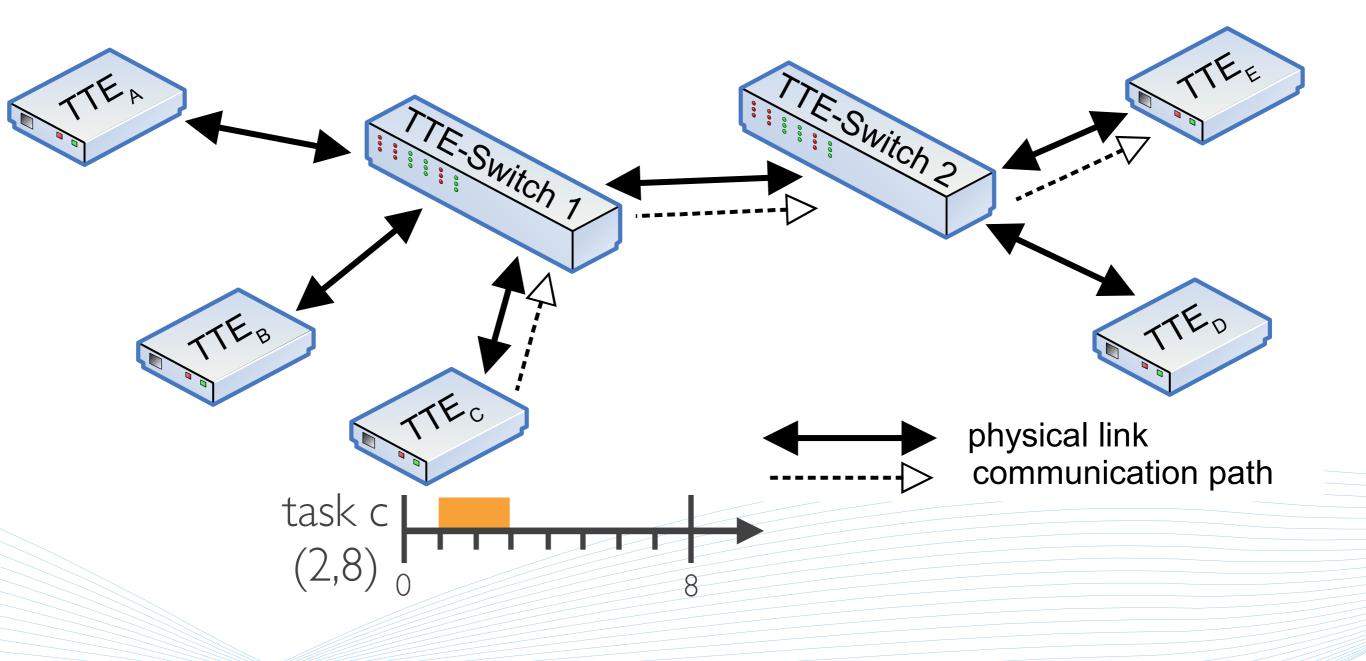




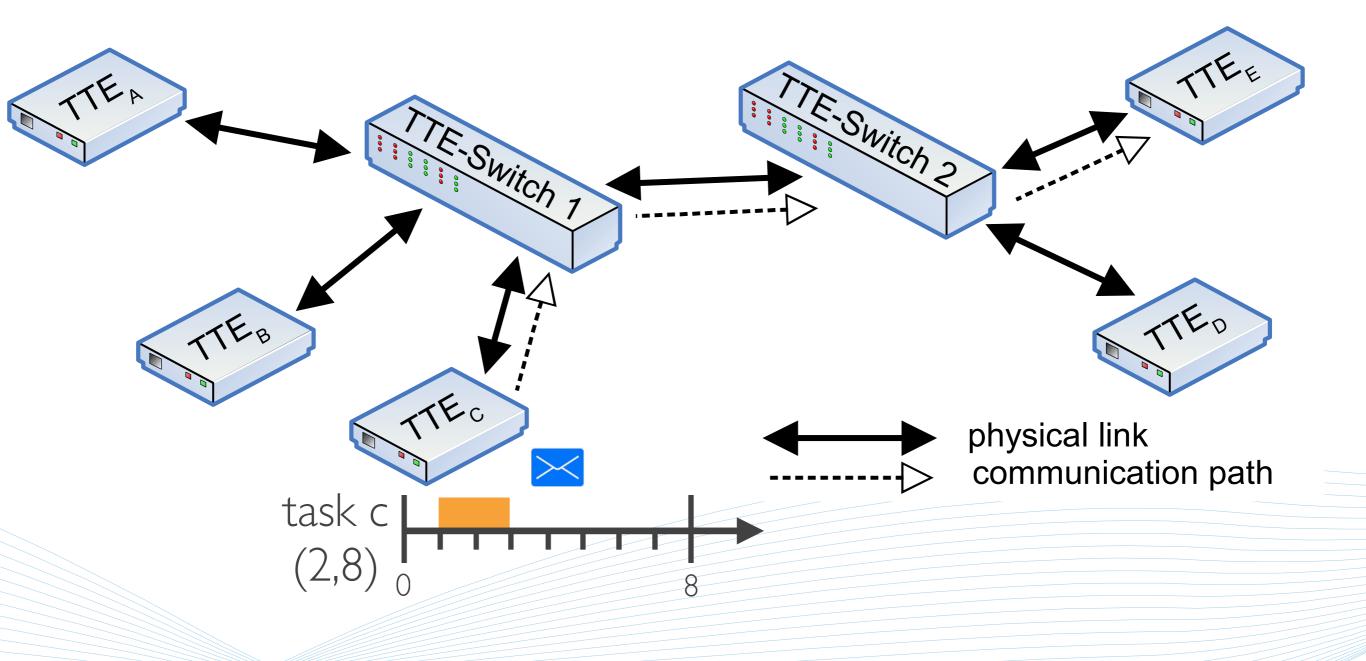
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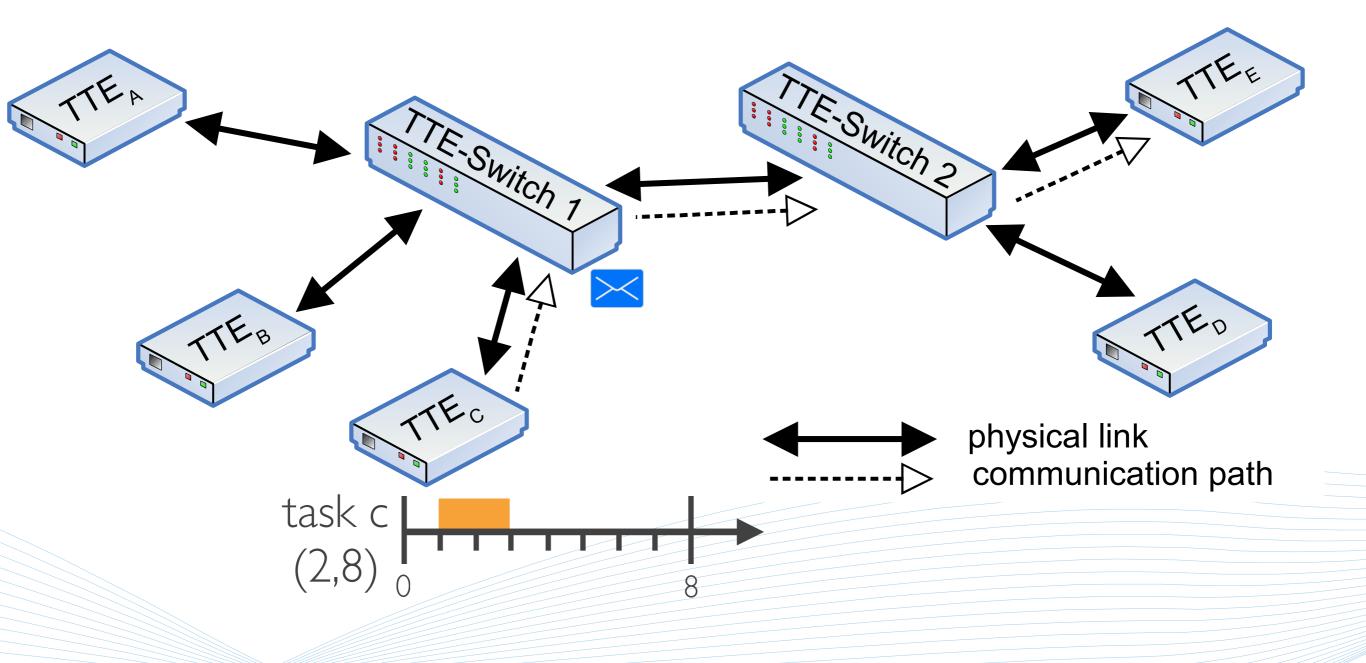
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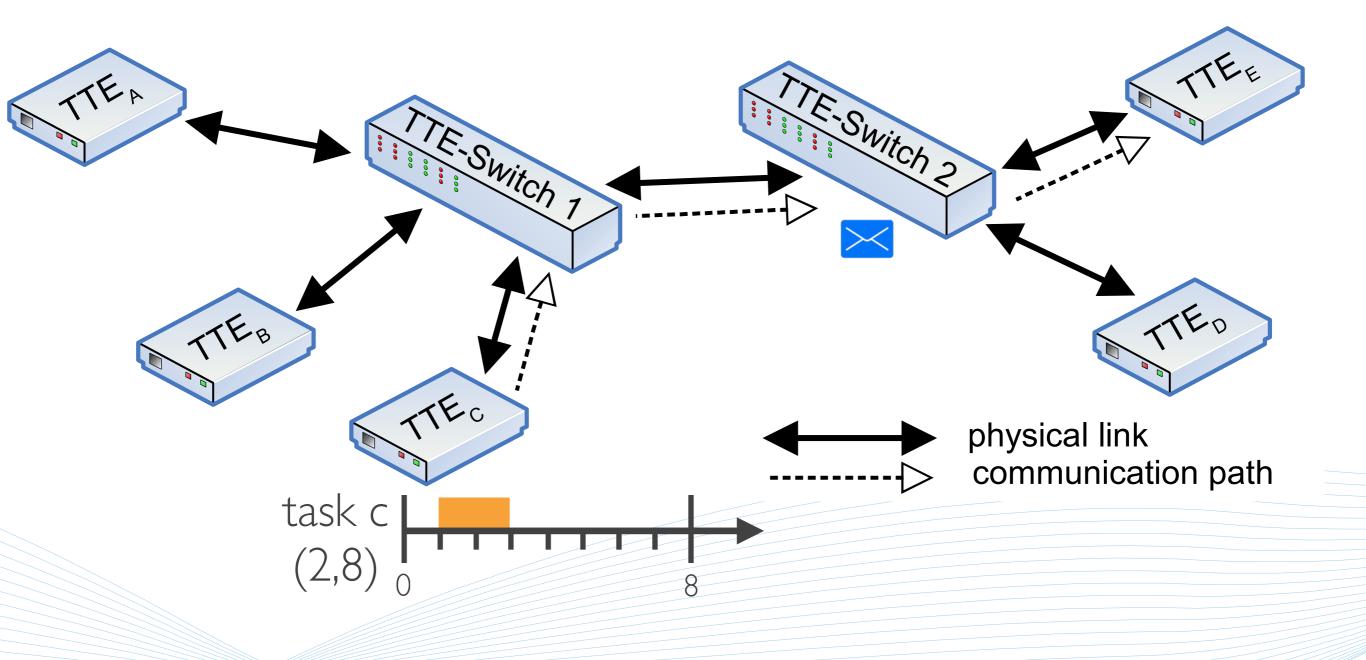
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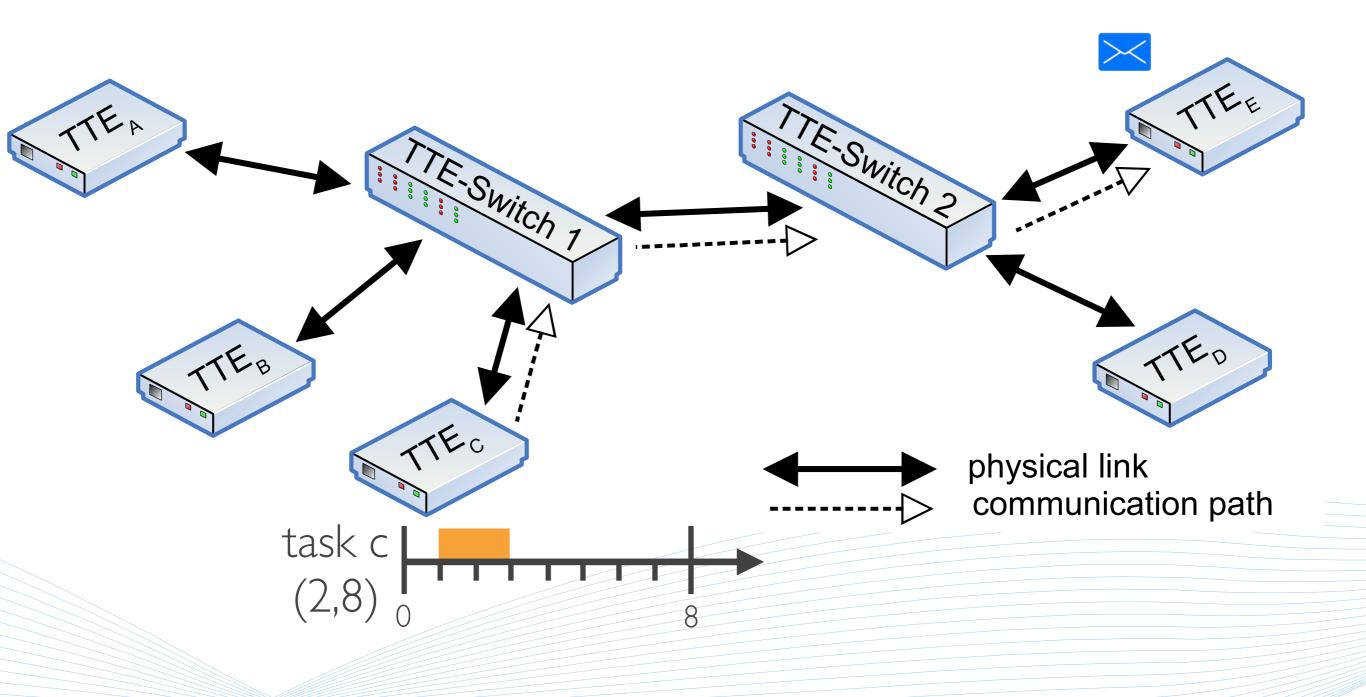
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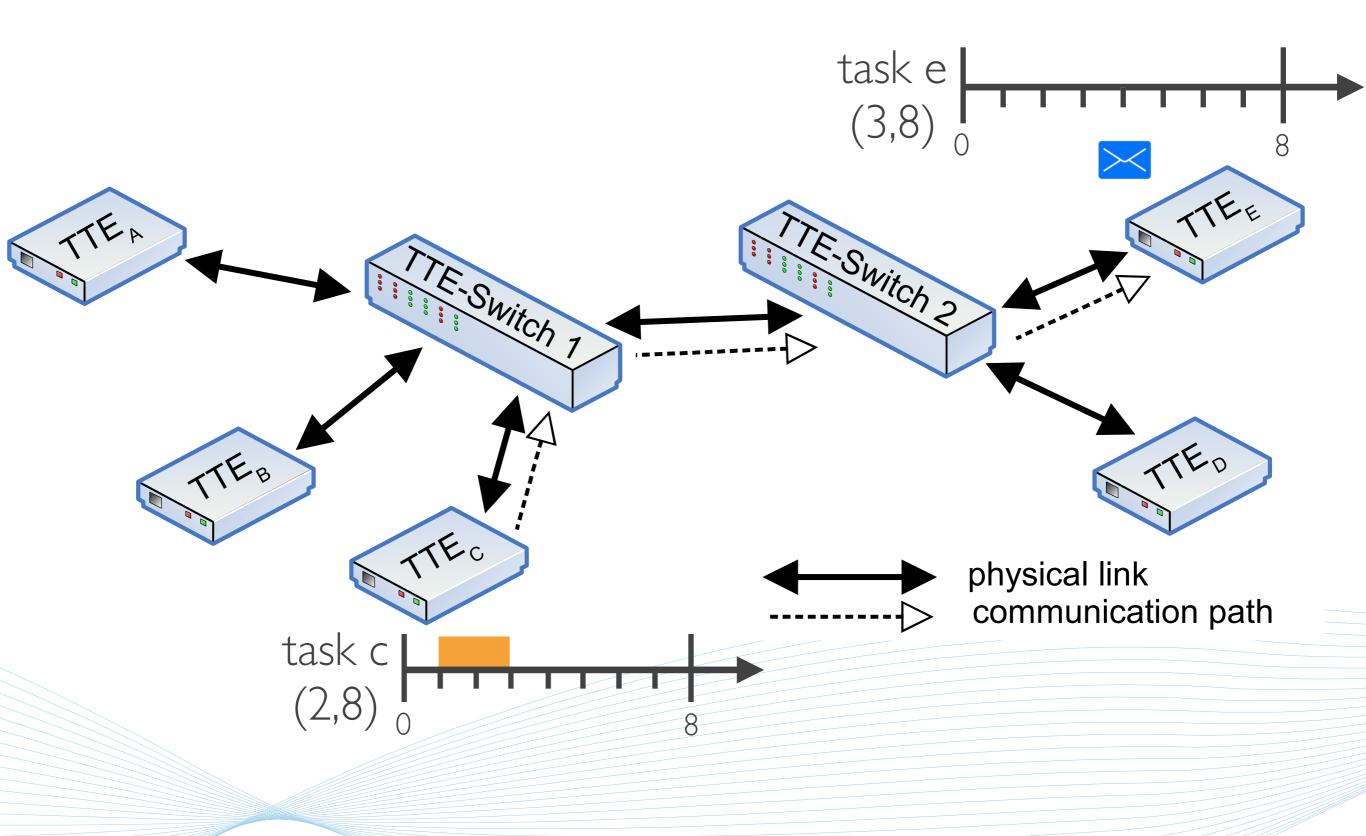
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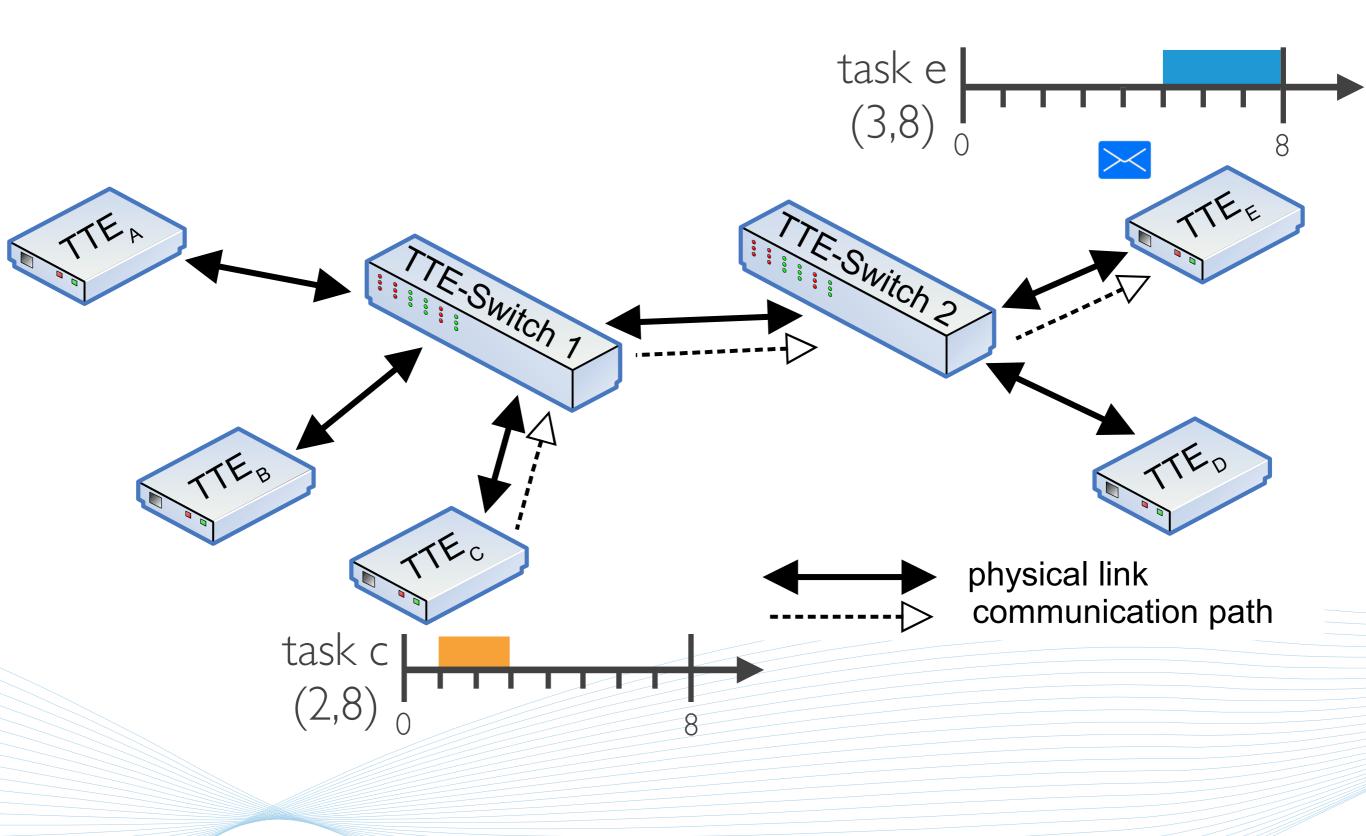
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Sequential scheduling

- Network [Steiner@RTSSI0] ▷ Tasks [Craciunas@ETFAI4]
- Tasks ▷ Network [Hanzalek@ECRTS09]

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Sequential scheduling

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- Tasks > Network [Hanzalek@ECRTS09]
- Combined scheduling

Network model

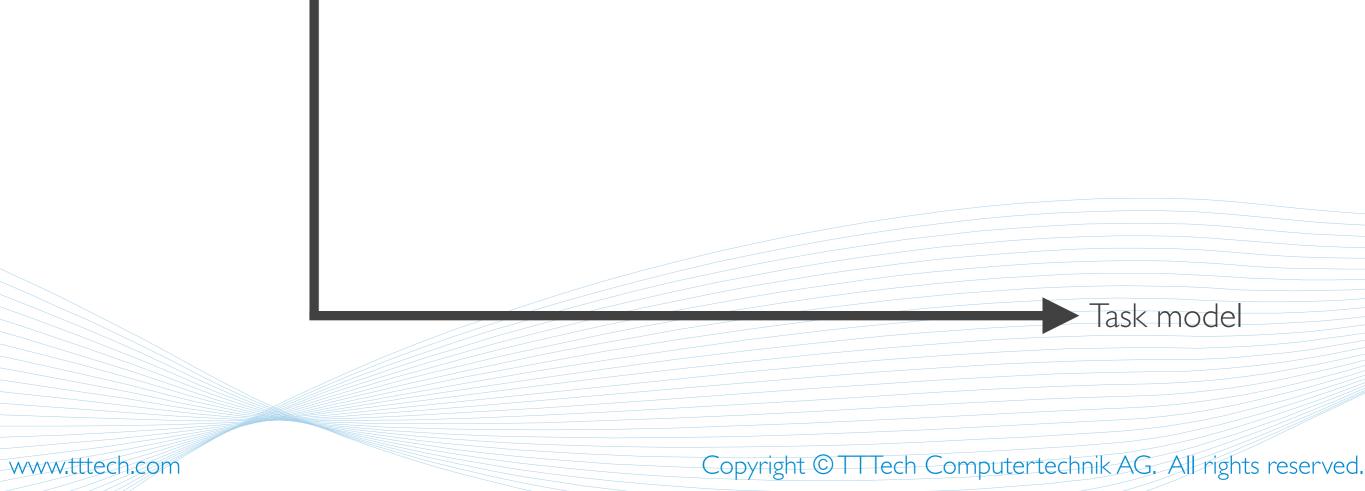
Task model

## Scheduling

Sequential scheduling

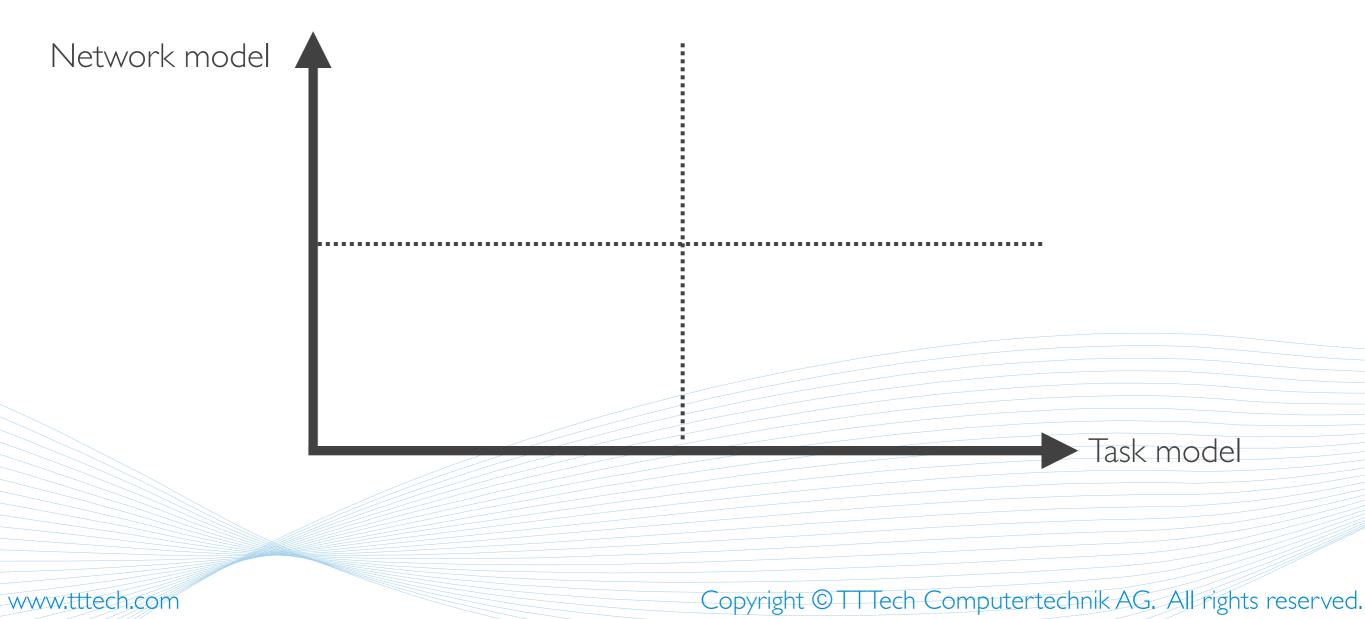
- Network [Steiner@RTSS10]  $\triangleright$  Tasks [Craciunas@ETFA14]
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Network model



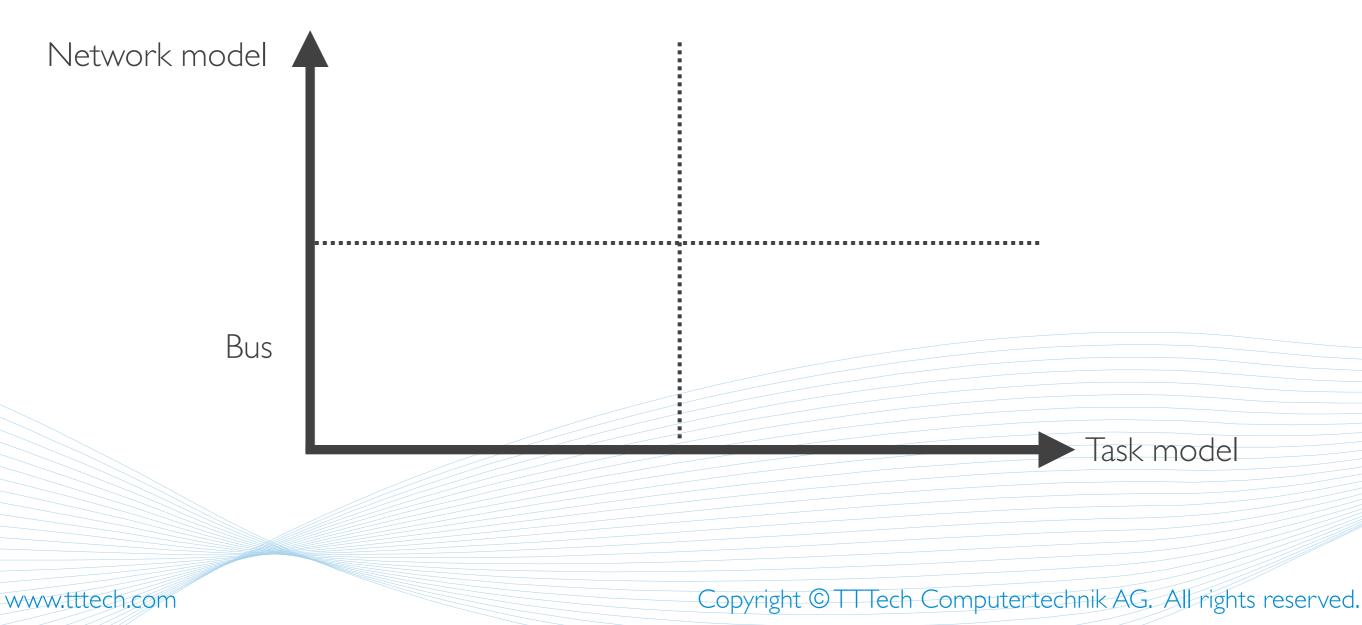
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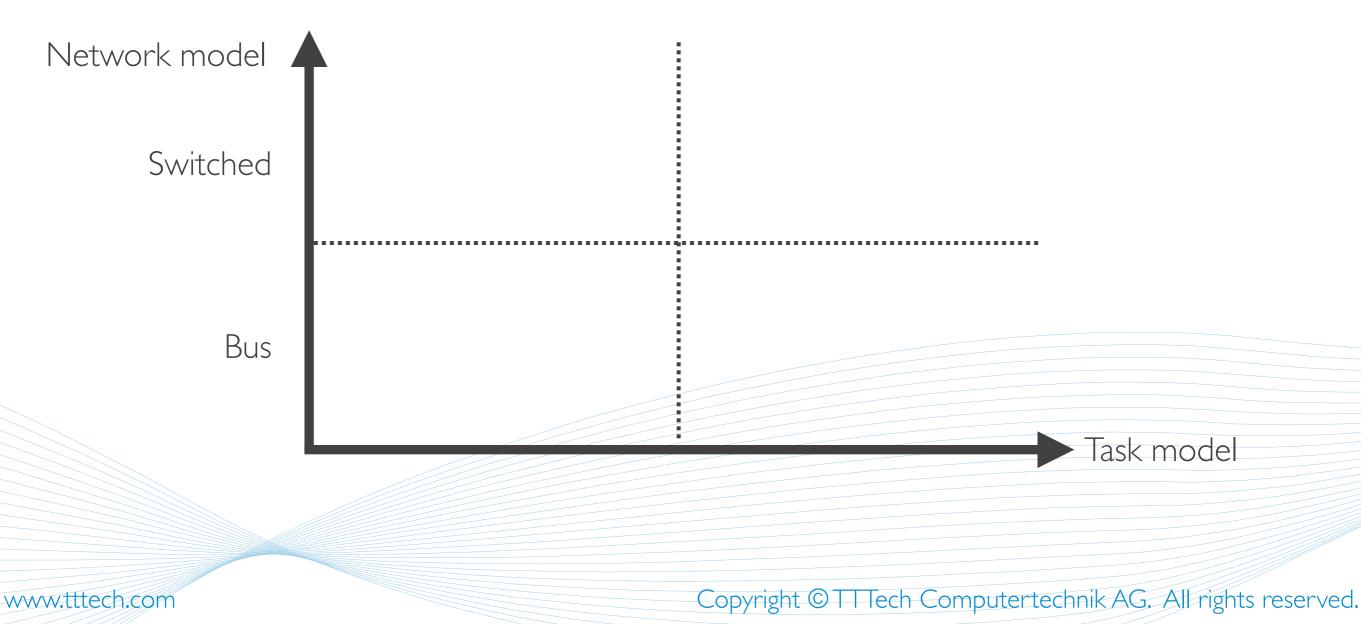
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- Network [Steiner@RTSSI0] ▷ Tasks [Craciunas@ETFAI4]
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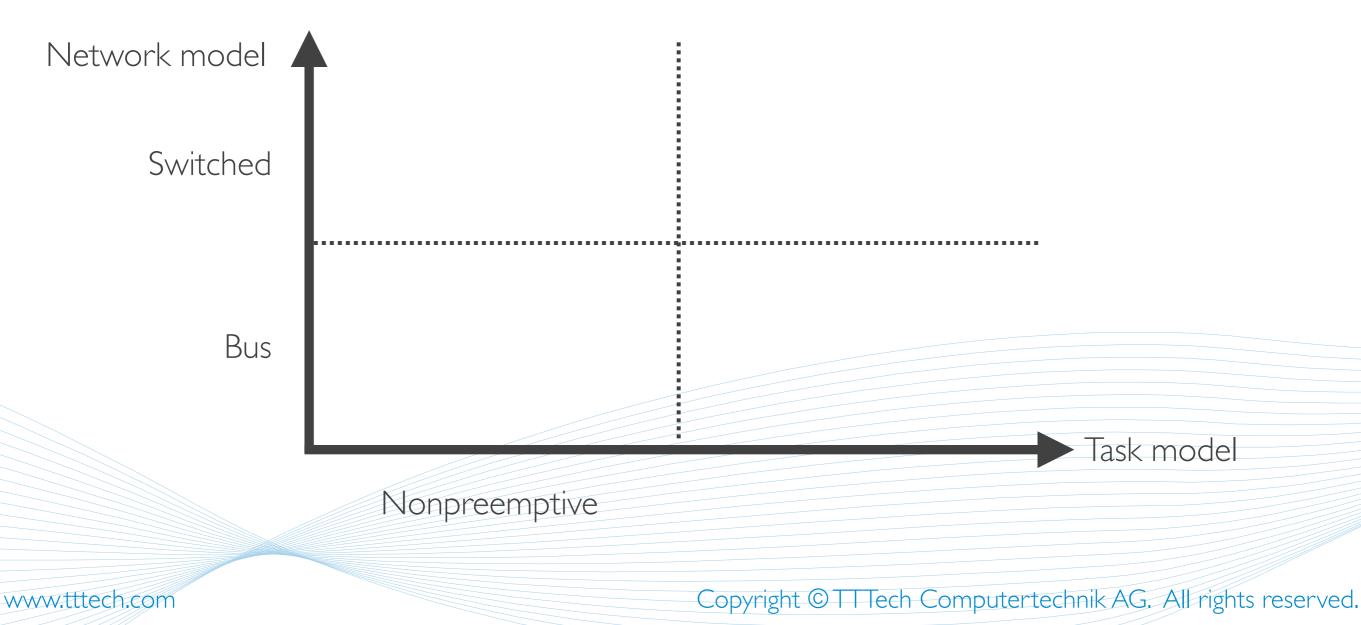
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- Network [Steiner@RTSSI0] ▷ Tasks [Craciunas@ETFAI4]
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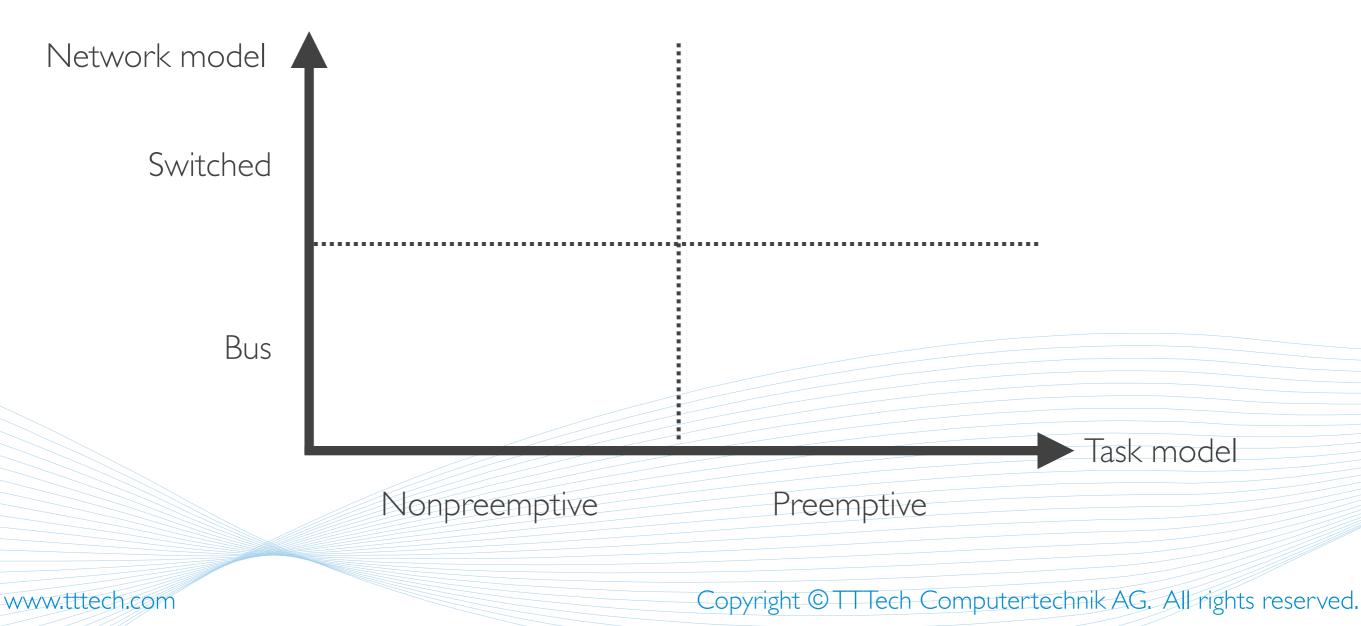
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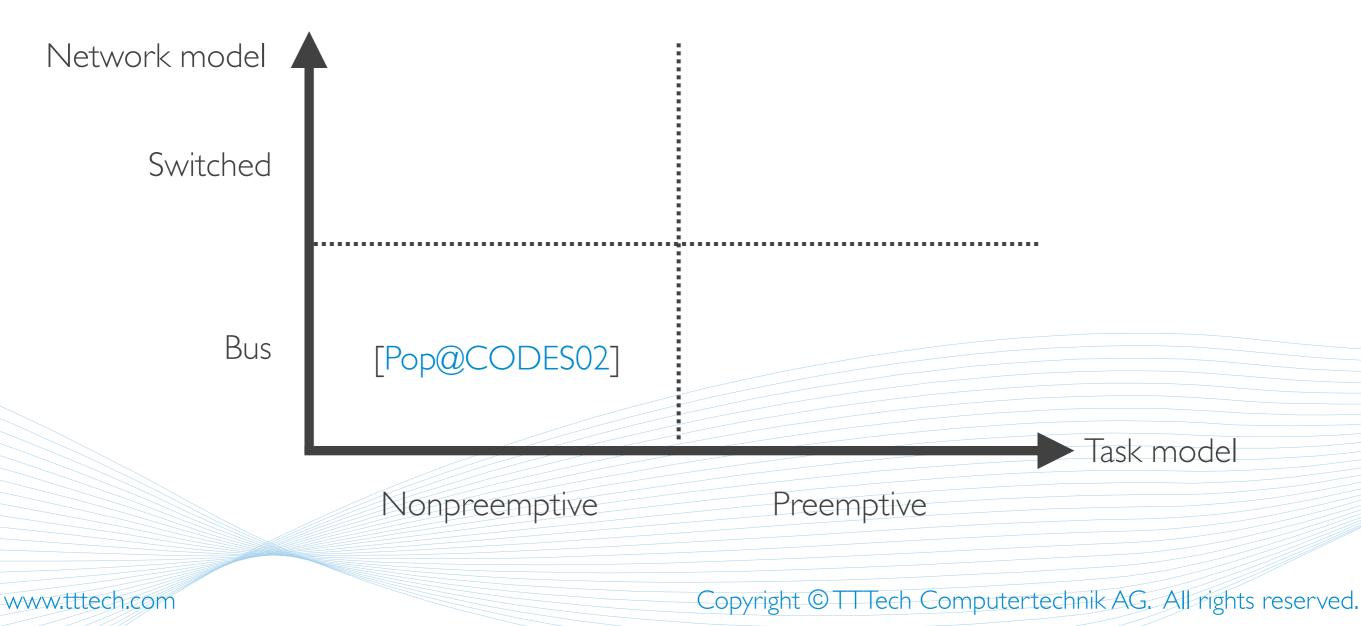
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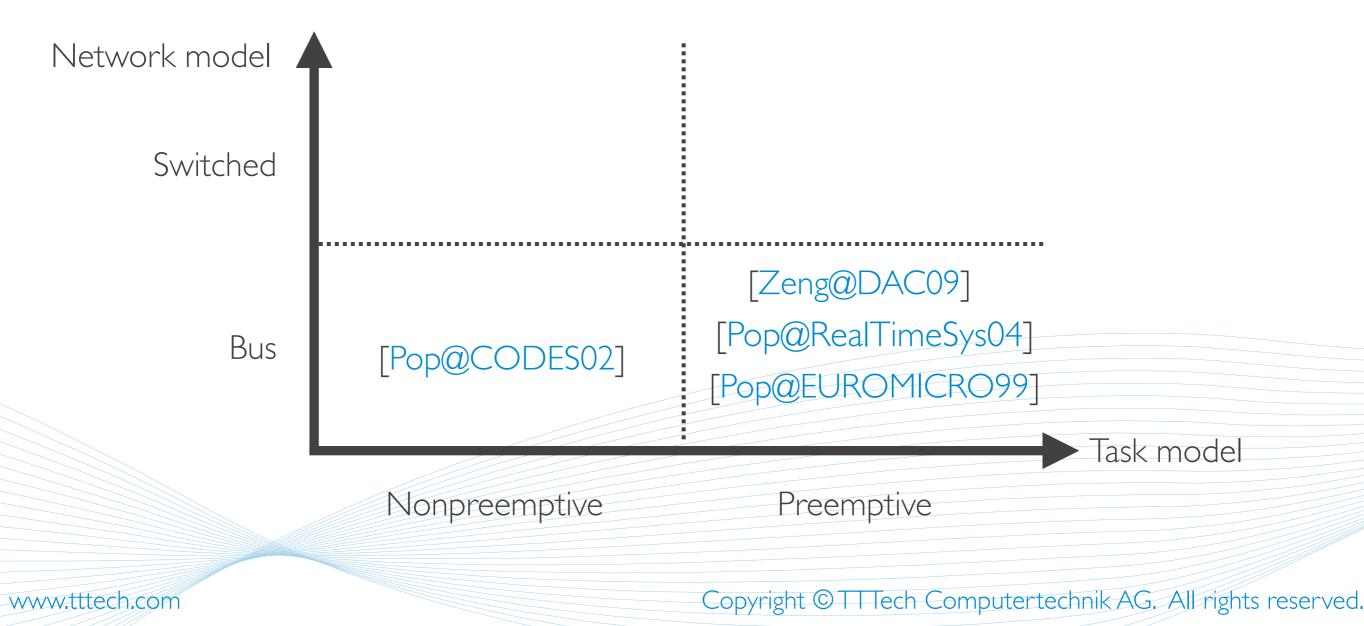
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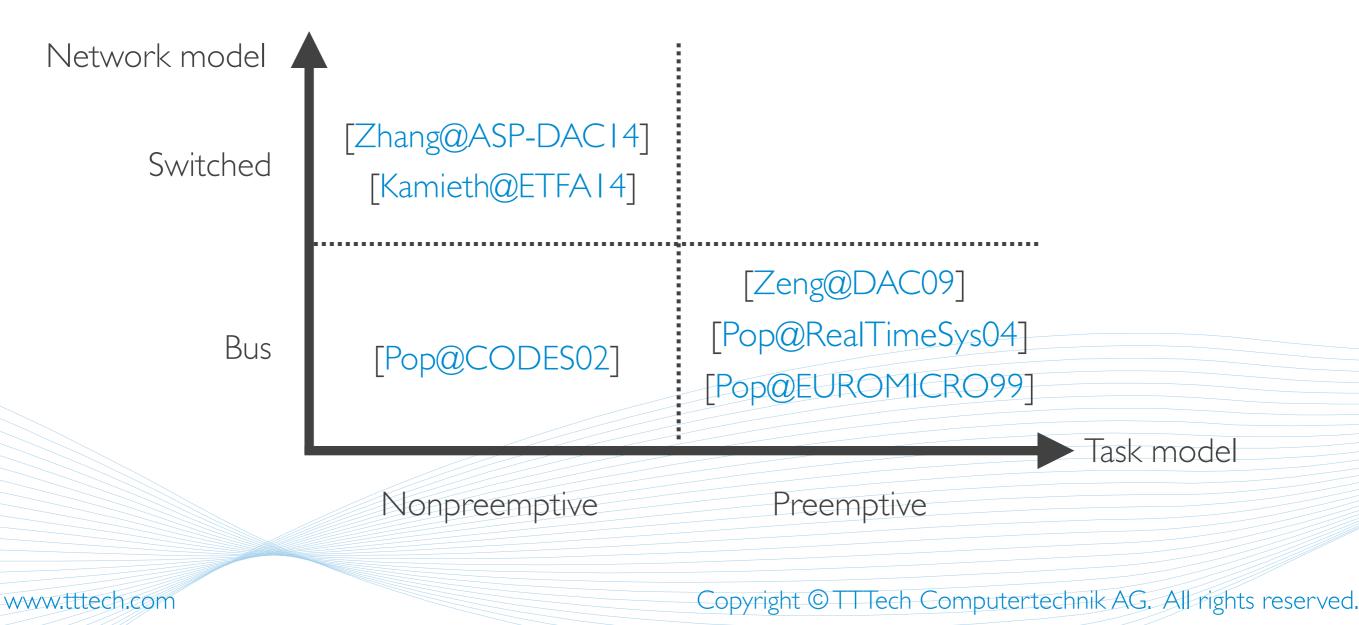
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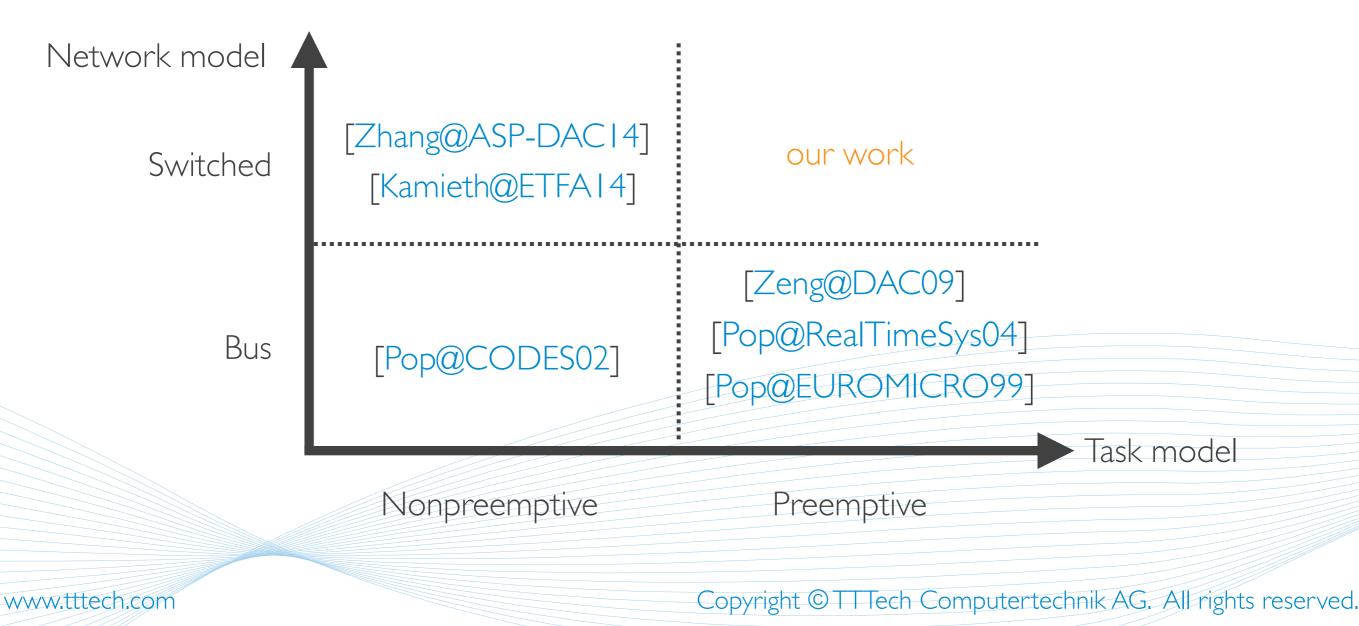
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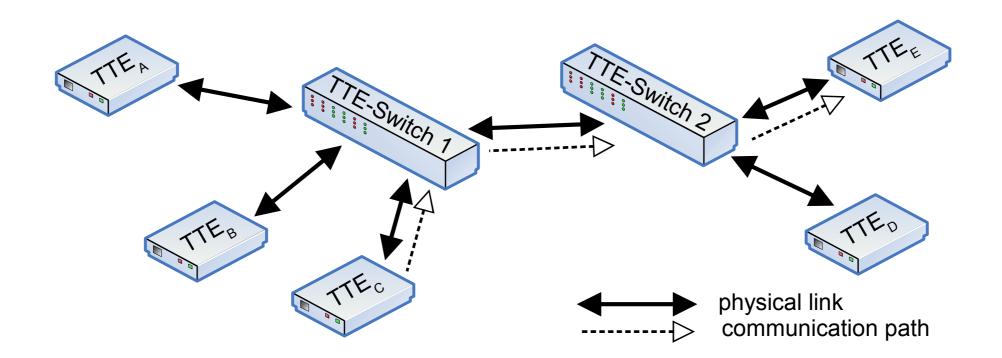
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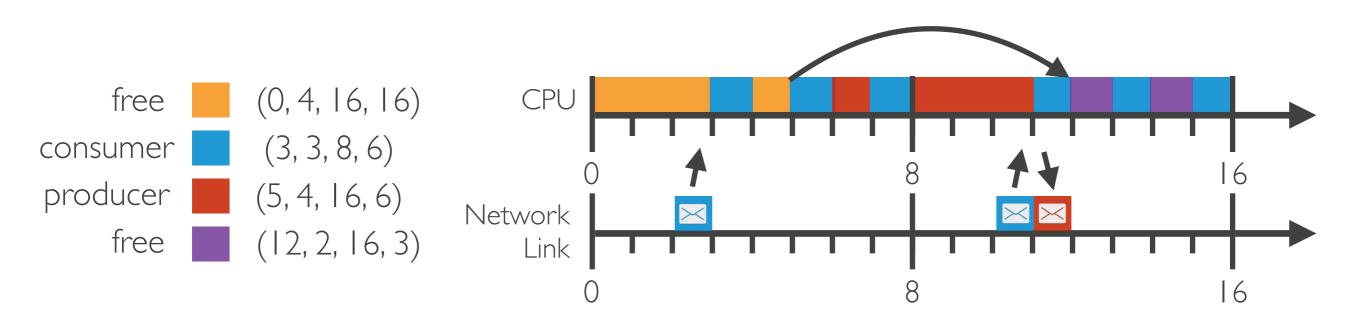
#### Network model



- multi-hop layer 2 switched network via full-duplex multi-speed links
- virtual links (ARINC 664 P-7)
- TT-traffic class (RC [Tamas-Selicean@CODES+ISSSI2], BE)
- synchronised time (< I used precision)</li>
- link delay for each link
- memory buffers on switches



#### Task model



- periodic asynchronous TT-tasks (offset  $\phi$  , weet C, period T, deadline D)
- static time-driven schedule with preemption
- 3 types of tasks (producer, consumer, free)
- macrotick on ES (usec ms)
- communication at beginning/end of consumer/producer ([Derler@CITI0])
- end-to-end latency, dependencies between tasks

#### Networked system model



Network

$$G(\mathcal{V}, \mathcal{L}) \quad \mathcal{L} \subseteq \mathcal{V} \times \mathcal{V}$$
$$\forall [v_a, v_b] \in \mathcal{L} \Rightarrow [v_b, v_a] \in \mathcal{L}$$

Network links 
$$\begin{bmatrix} v_a, v_b \end{bmatrix}$$
 (speed, link delay, macrotick, memory buffer)  
CPU self-links  $\begin{bmatrix} v_a, v_a \end{bmatrix}$ 

Virtual link - dataflow from one producer to one receiver  $vl_i = [[v_a, v_a], [v_a, v_1], [v_1, v_2], \dots, [v_{n-1}, v_n], [v_n, v_b], [v_b, v_b]].$ 

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#### Frames



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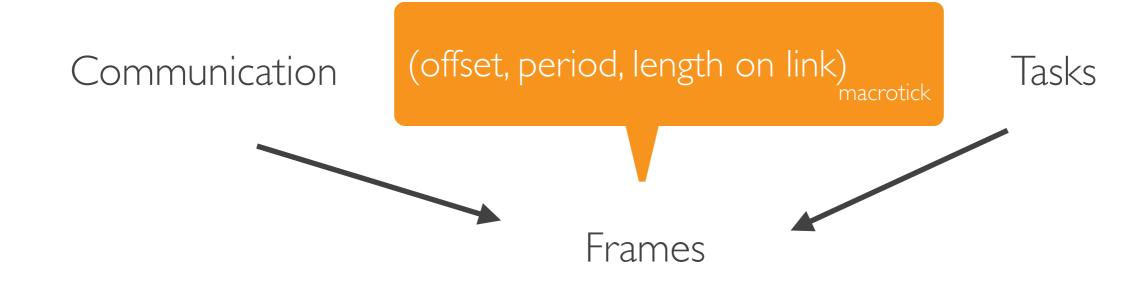
Communication



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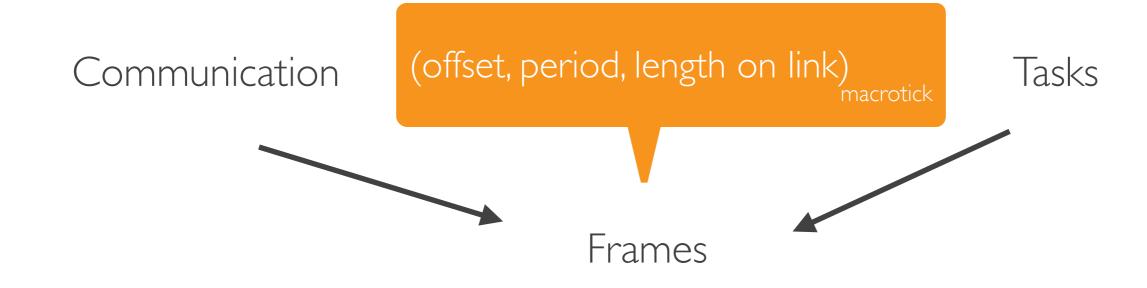




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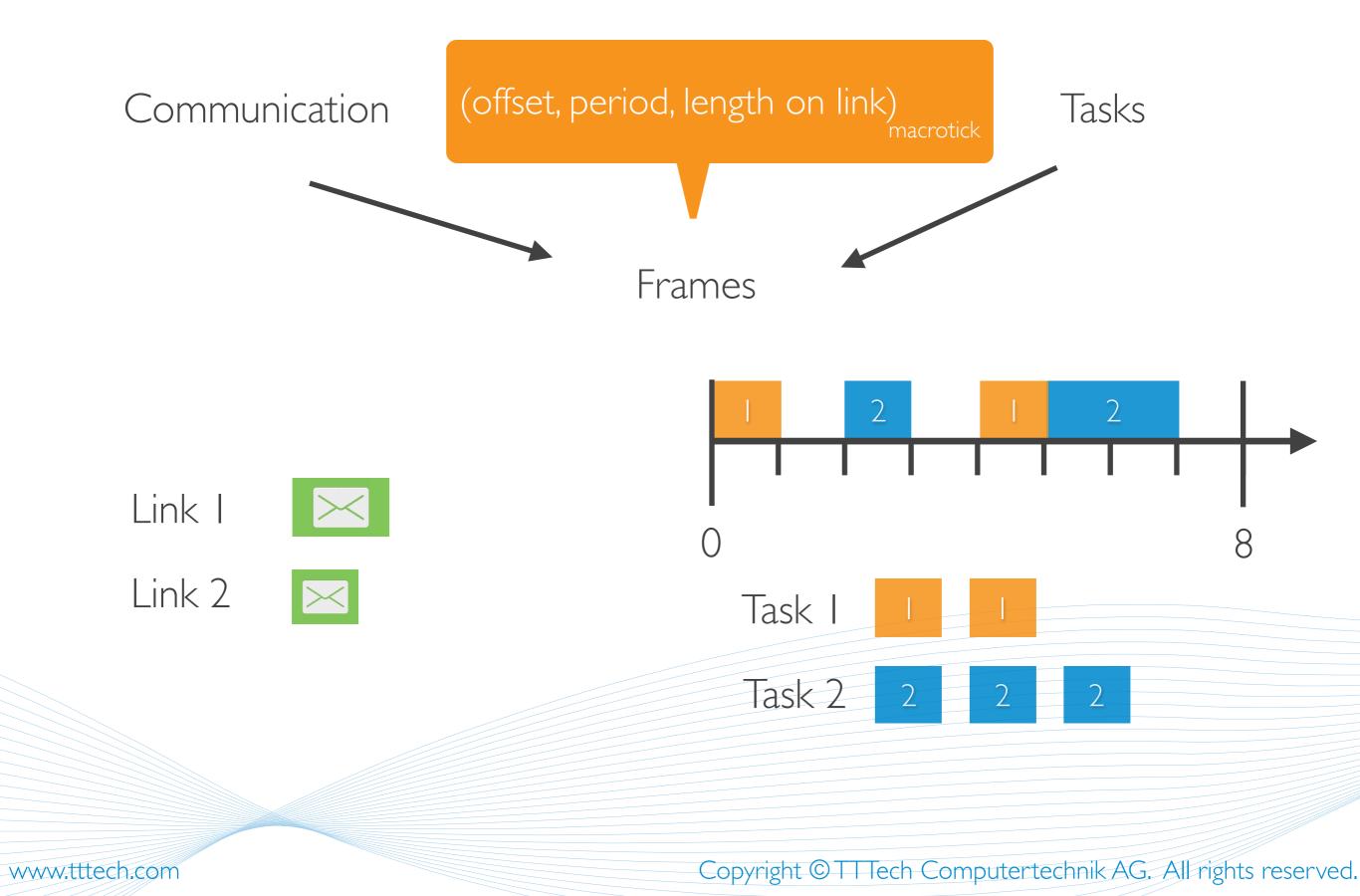






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#### Scheduling problem



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#### Scheduling problem

find offsets for the frames (on links and virtual task frames)

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reduces to finding a solution for a set of constraints

- frame constraints
- link constraints
- virtual link constraints
- memory constraints
- end-to-end latency constraints
- precedence constraints

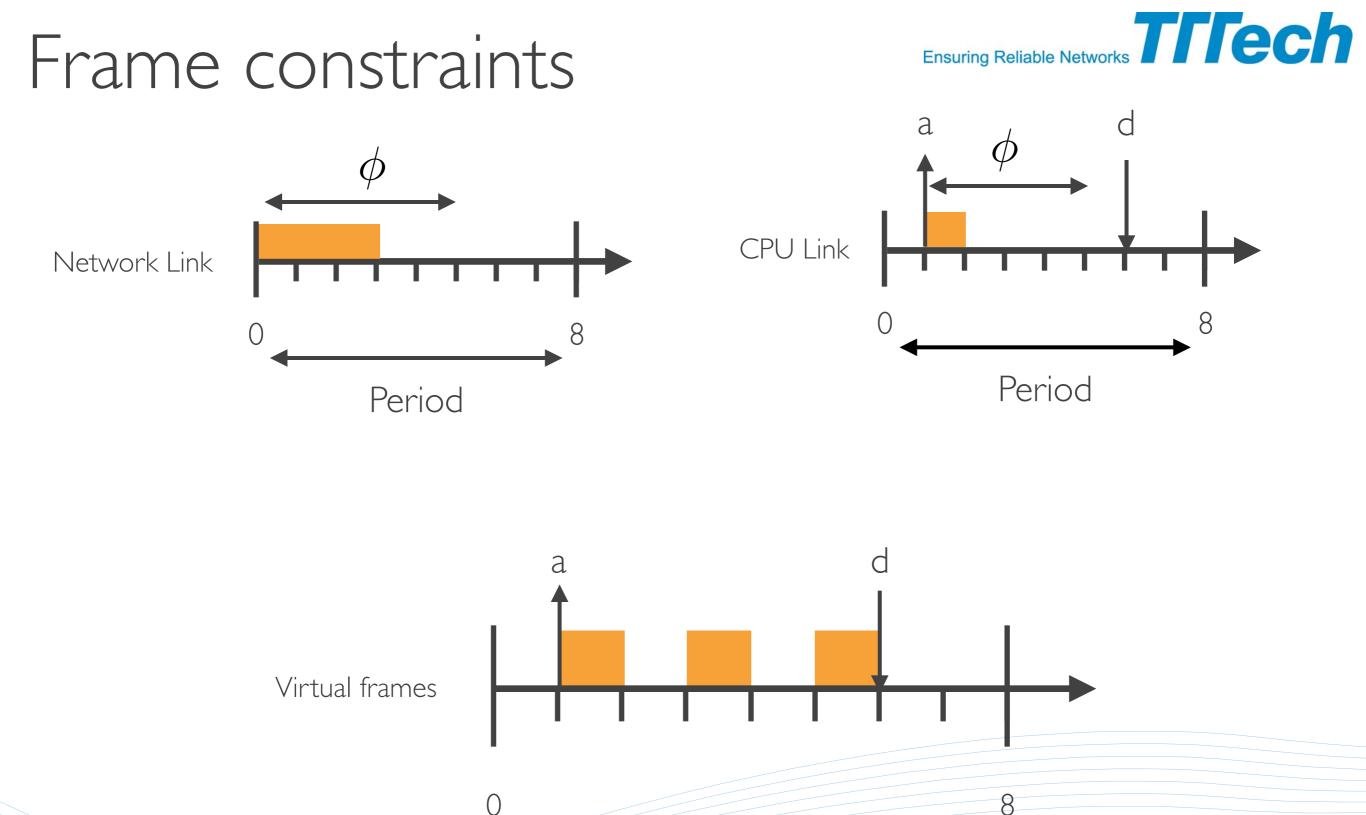
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#### NP-complete

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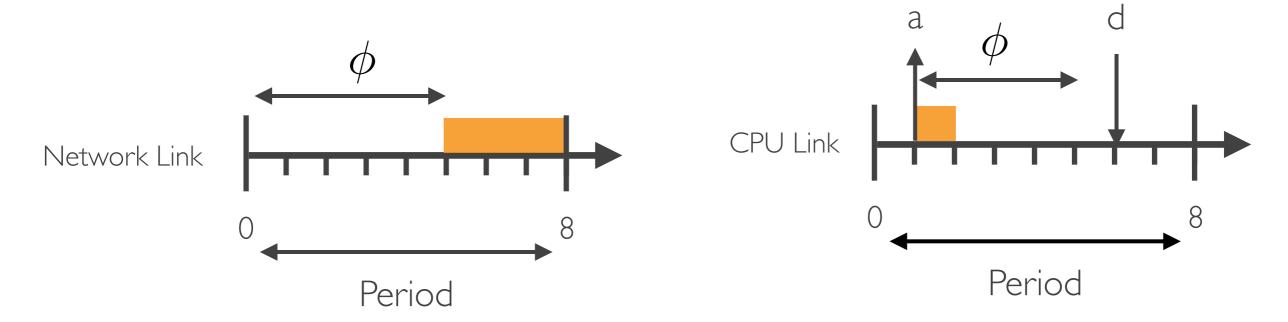


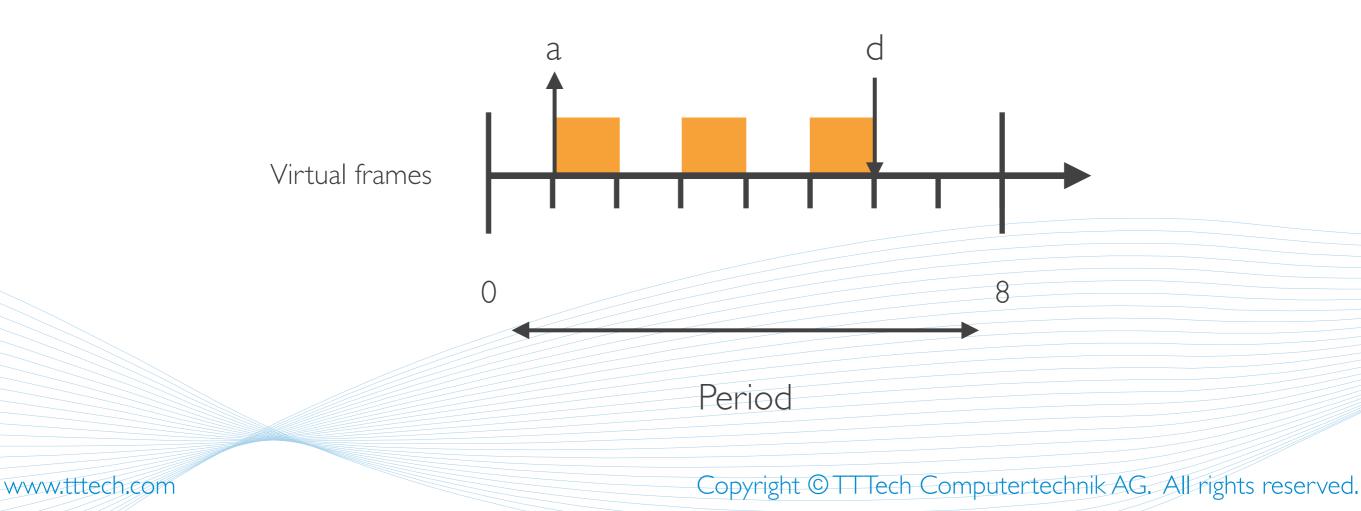
Period

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## Frame constraints

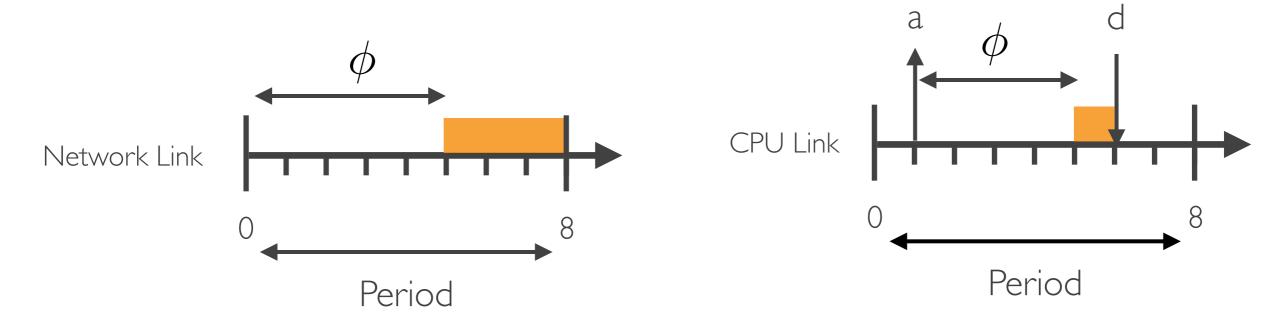


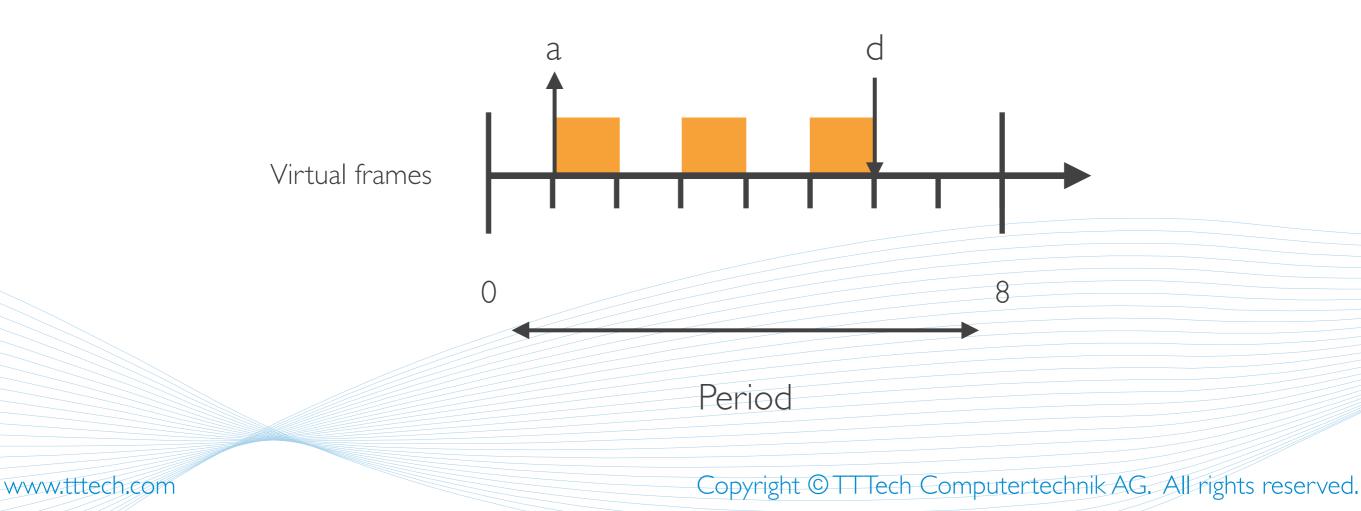




# Frame constraints

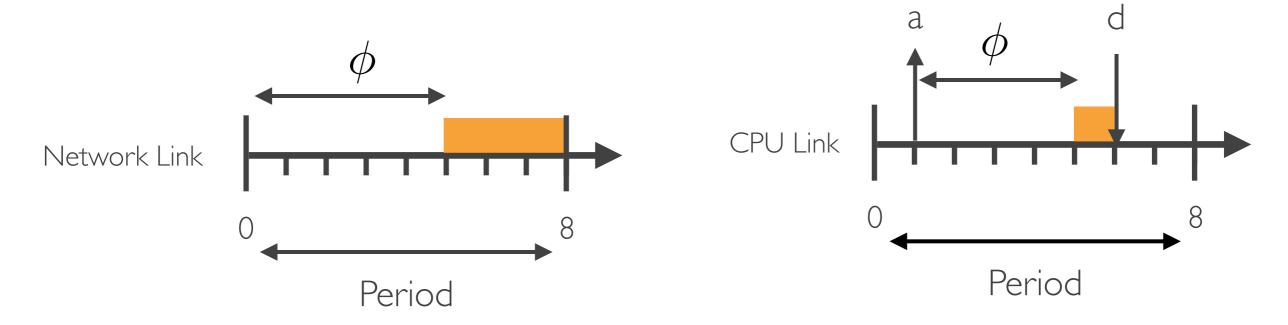


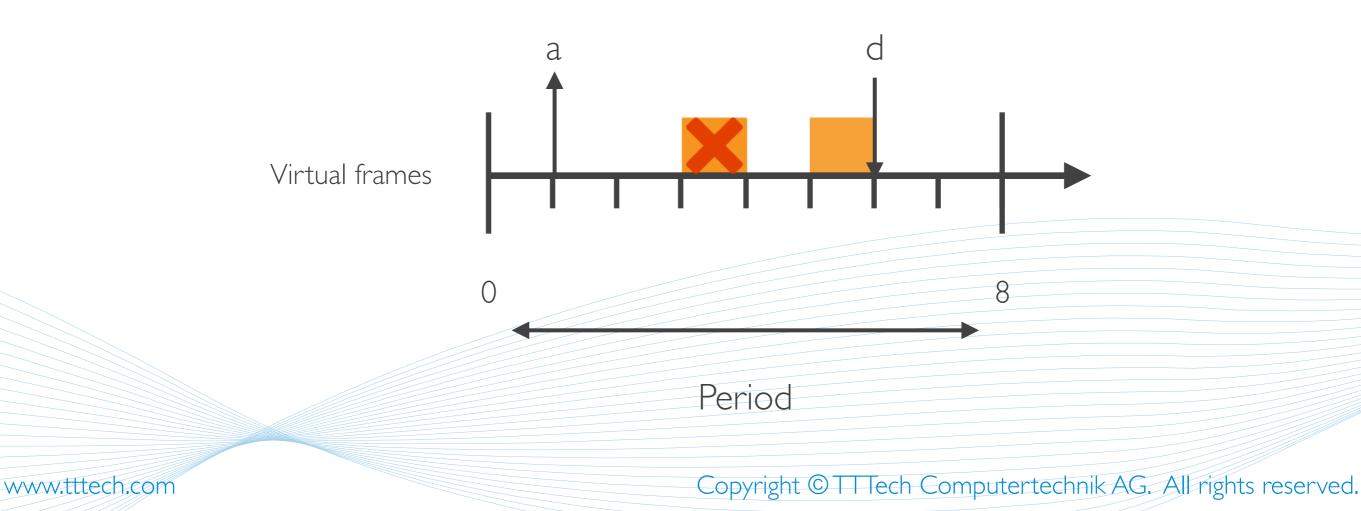




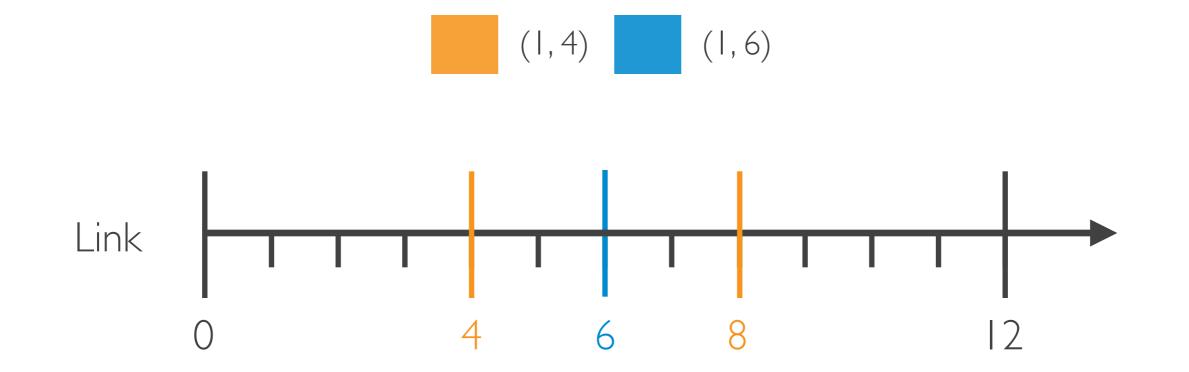
# Frame constraints





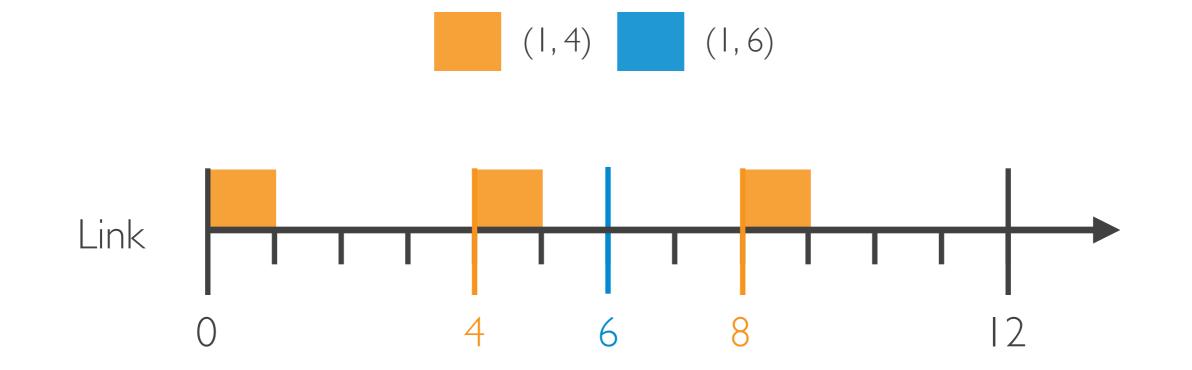






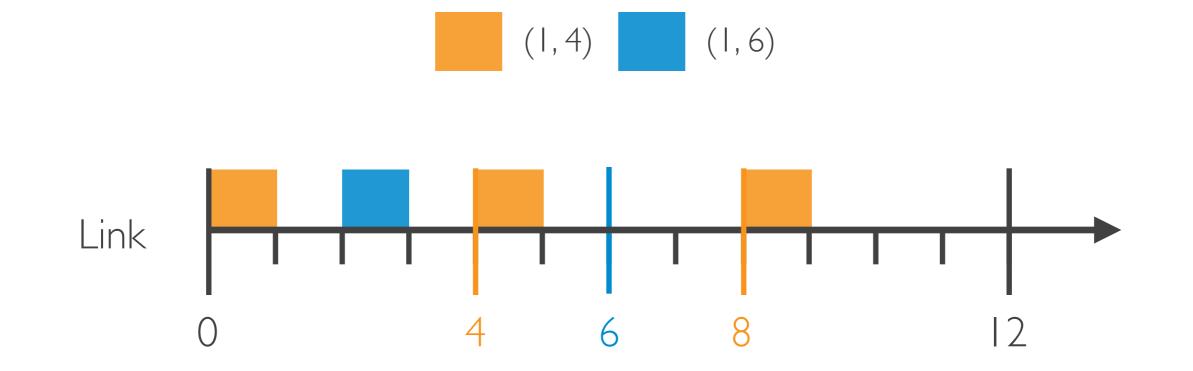
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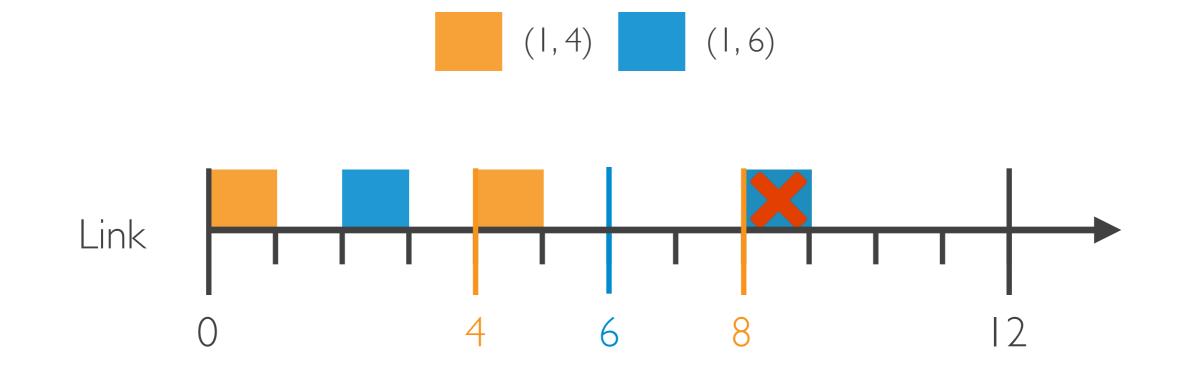


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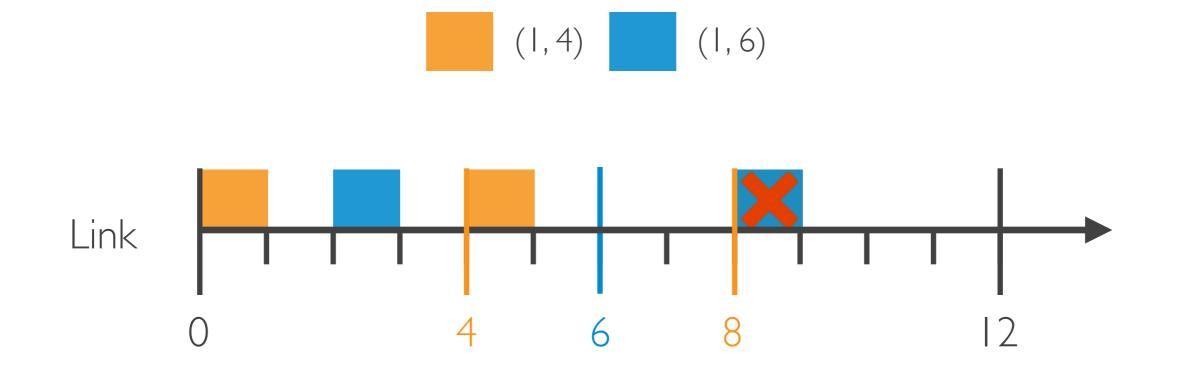




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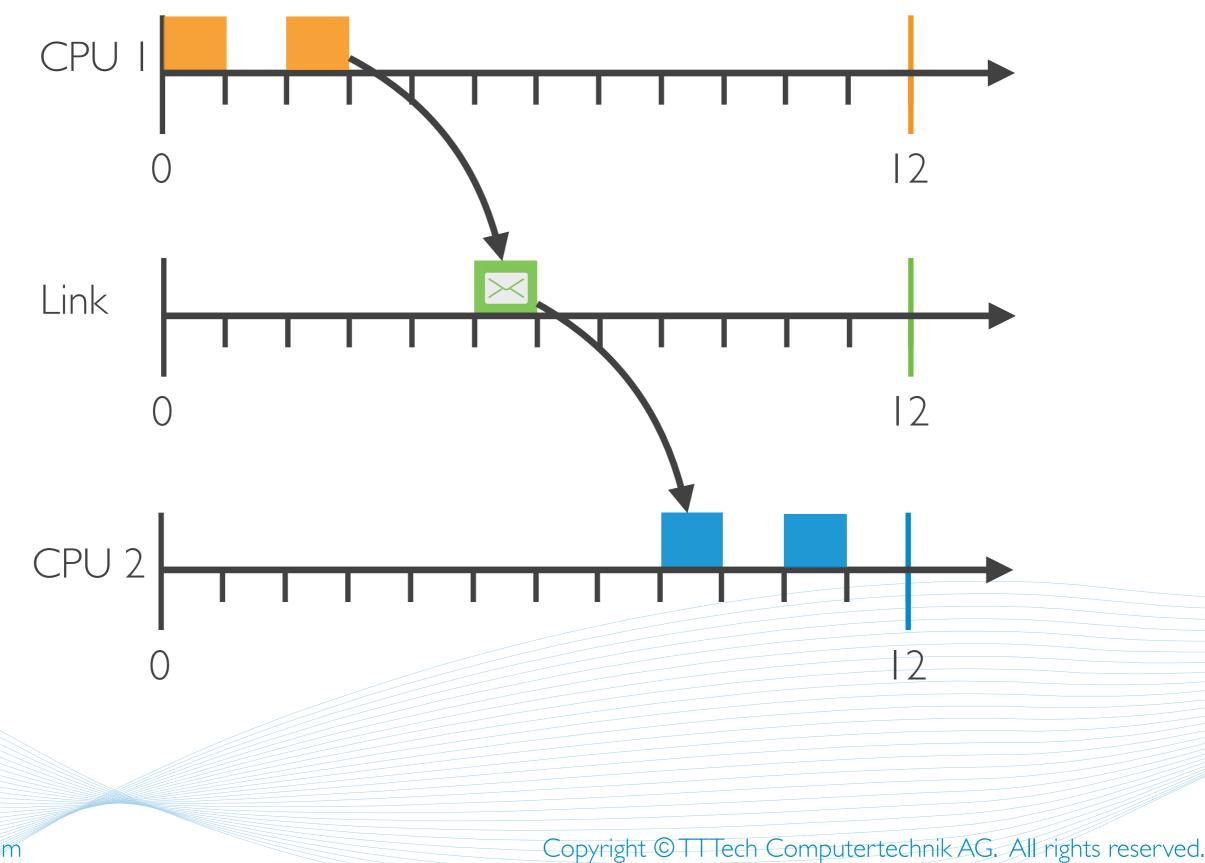




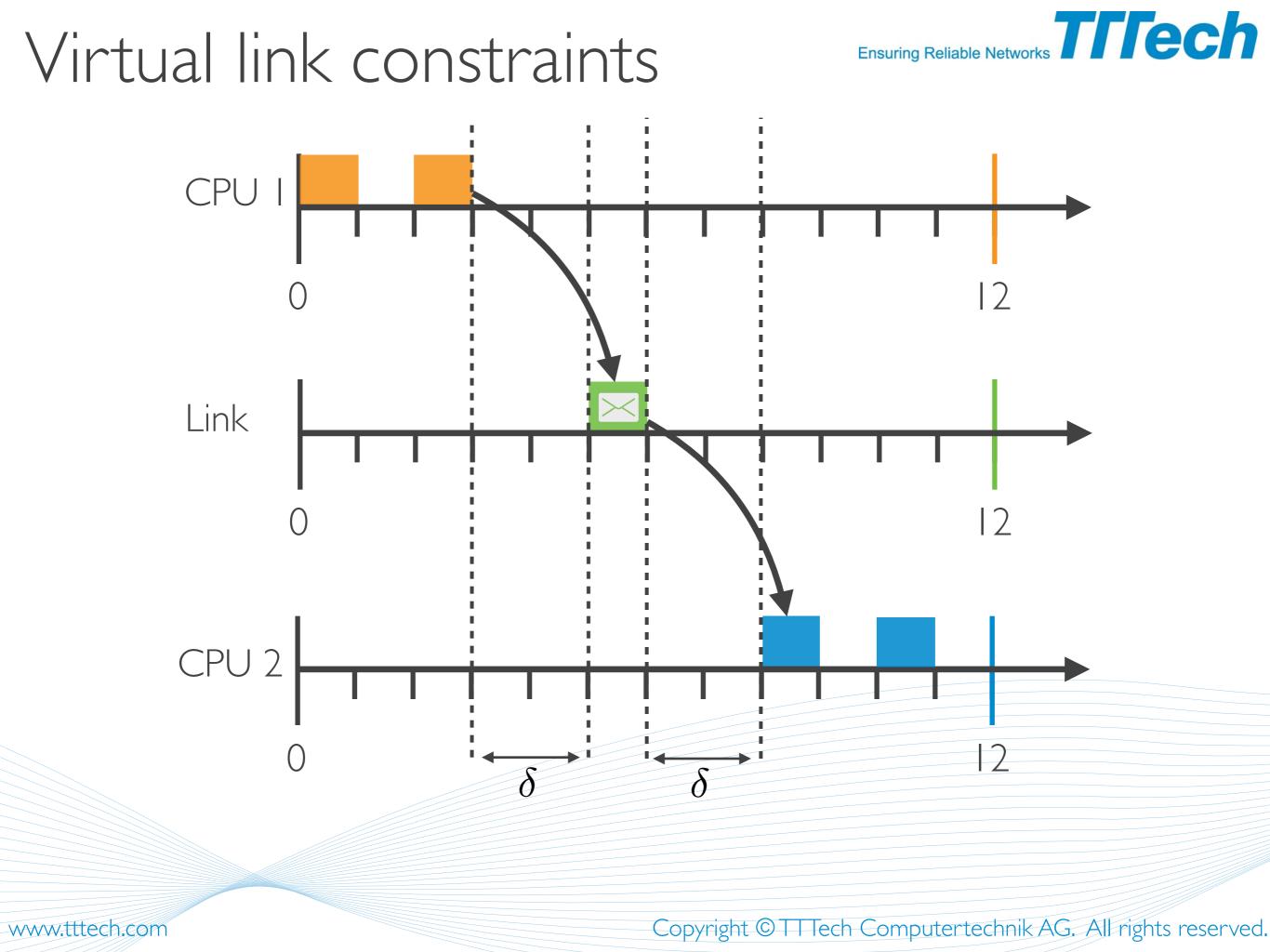
no two frames scheduled on the same link may overlap

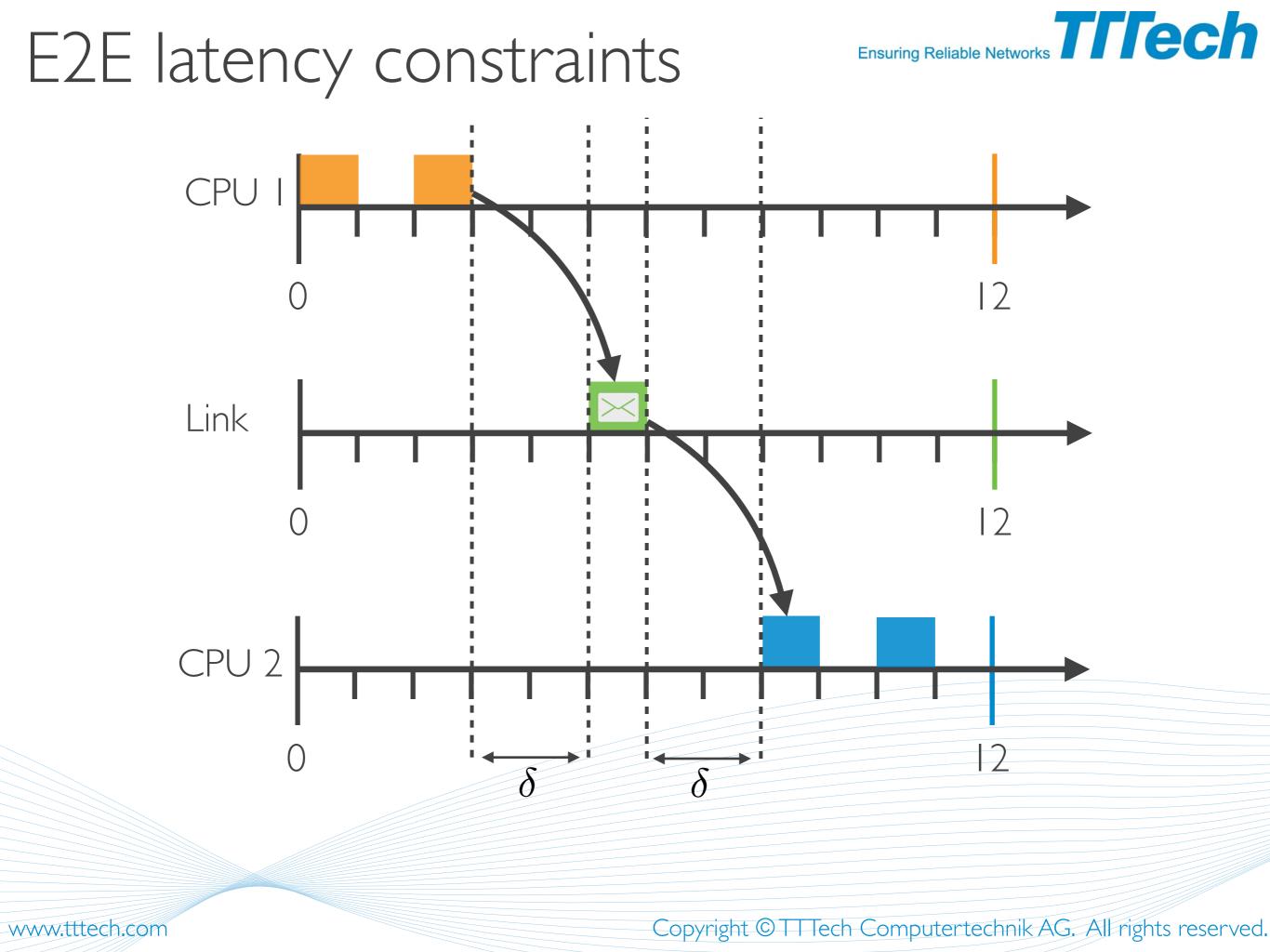


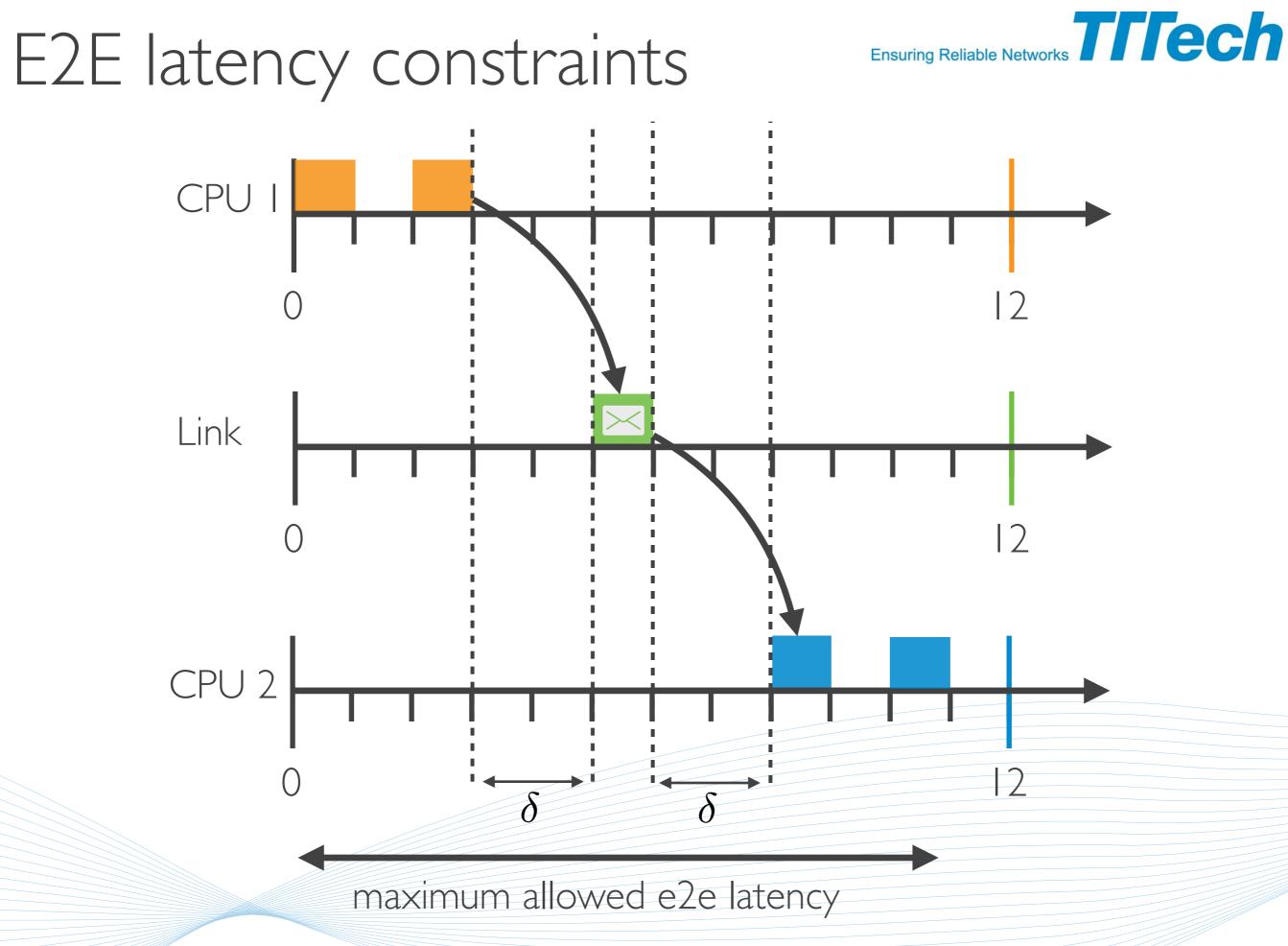
# Virtual link constraints



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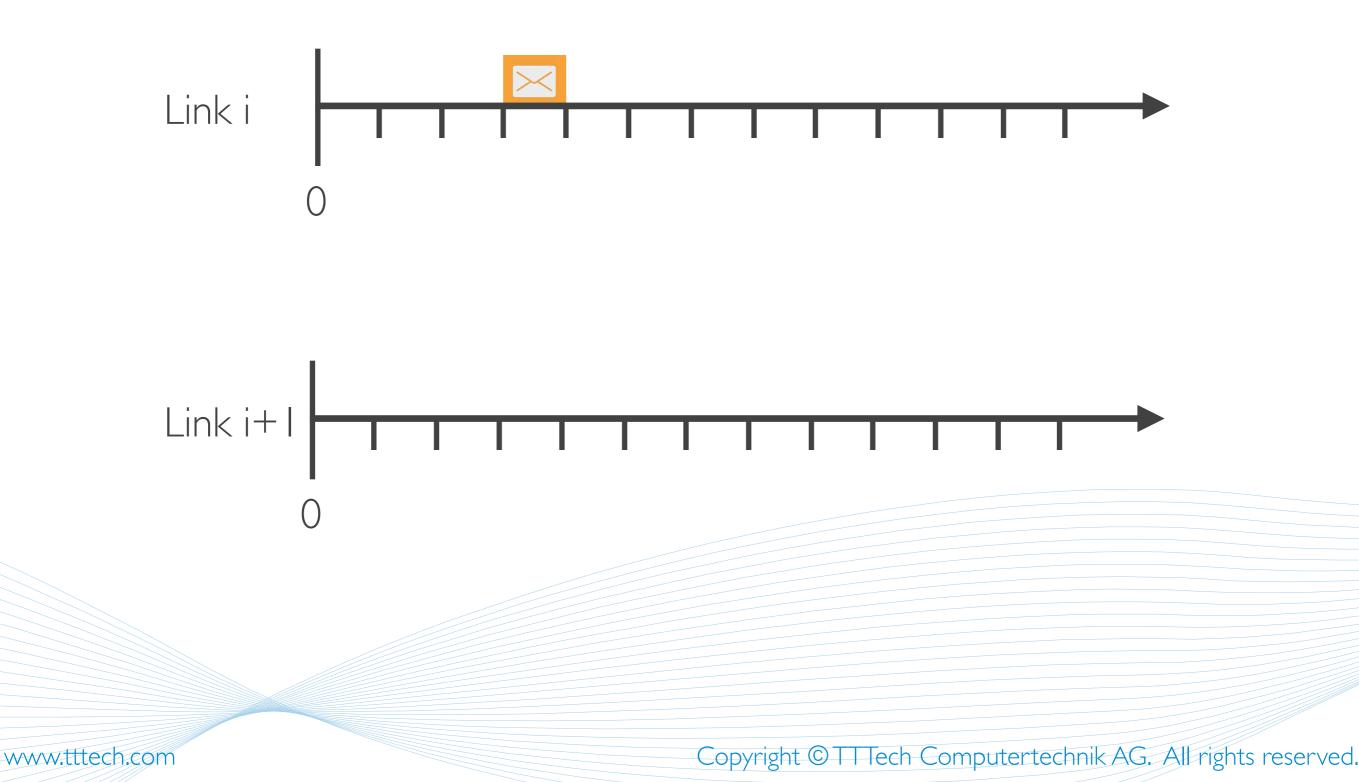




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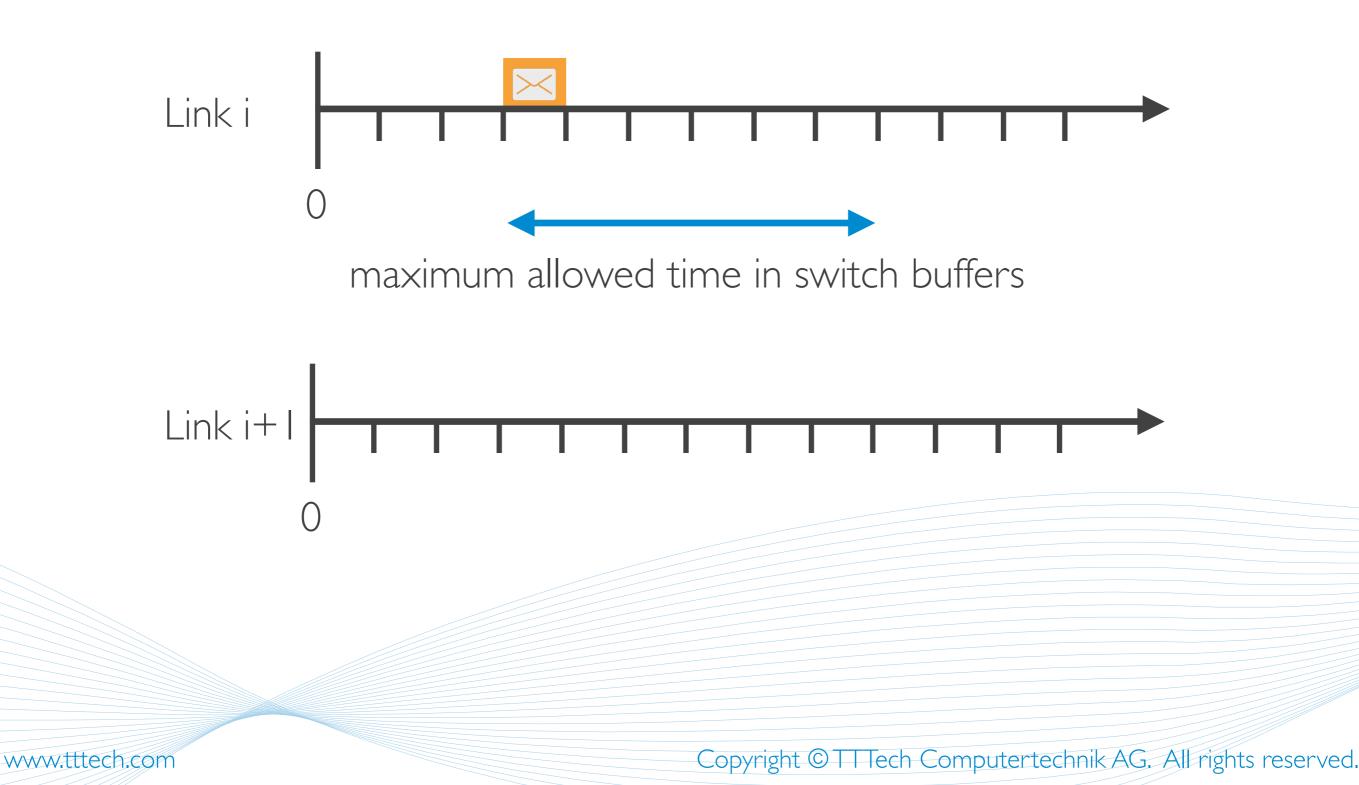


# Memory constraints



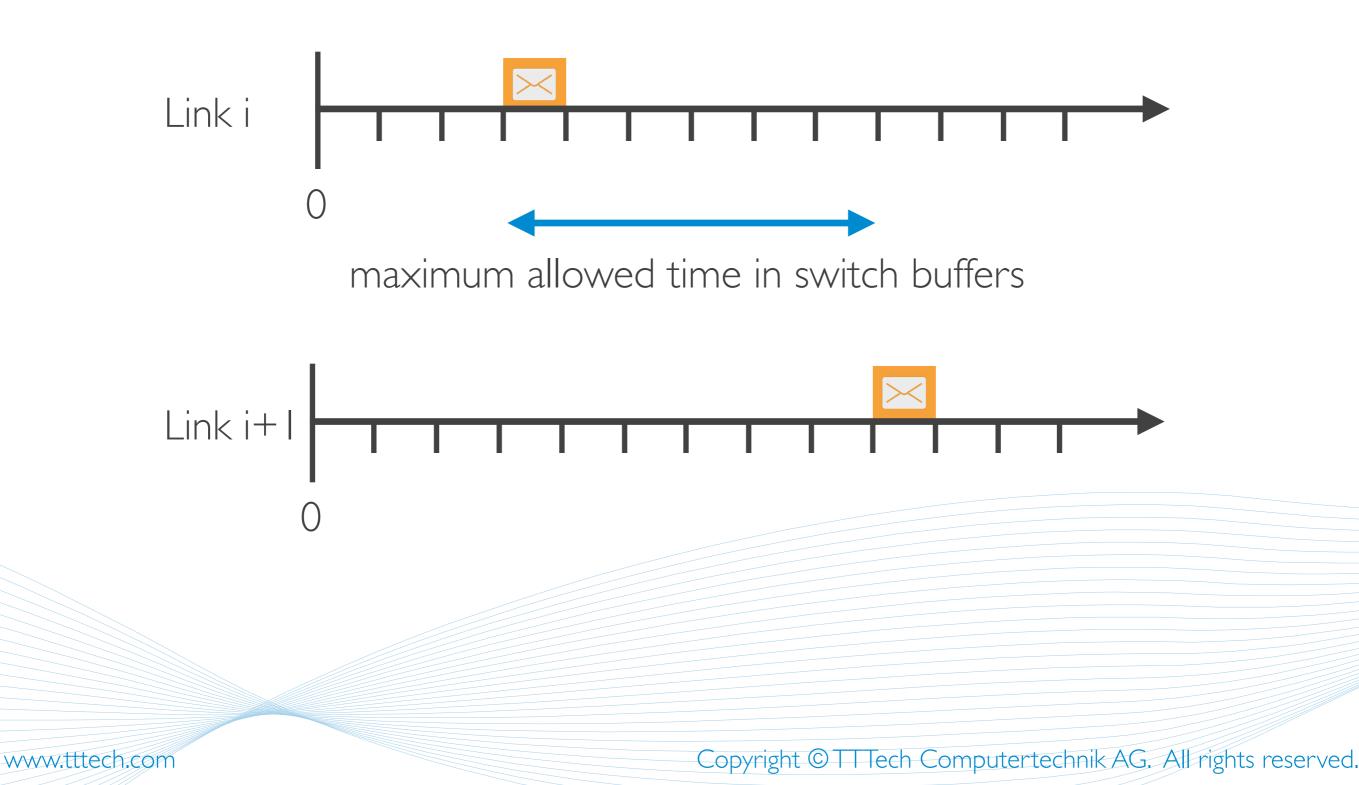


# Memory constraints





# Memory constraints





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satisfiability of logical formulas in first-order formulation

background theories  $\mathcal{LA}(\mathbb{Z}) \ \mathcal{BV}$ 

variables  $x_1, x_2, \ldots, x_n$ 

logical symbols  $\vee, \wedge, \neg, (,)$ 

non-logical symbols  $+, =, \%, \leq$ 

quantifiers  $\exists, \forall$ 



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A lot of solvers and a very active community

OpenSMT [Bruttomesso@TACAS10] Yices Dutertre@CAV14 CVC4 [Barrett@CAVII] Z3 [de Moura@TACAS08]

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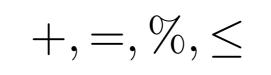


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$$\land, \neg, (, \neg)$$

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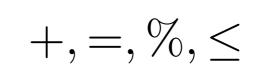


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quantifiers  $\exists d d d$ 



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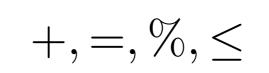


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$$, \wedge, \neg, (,)$$

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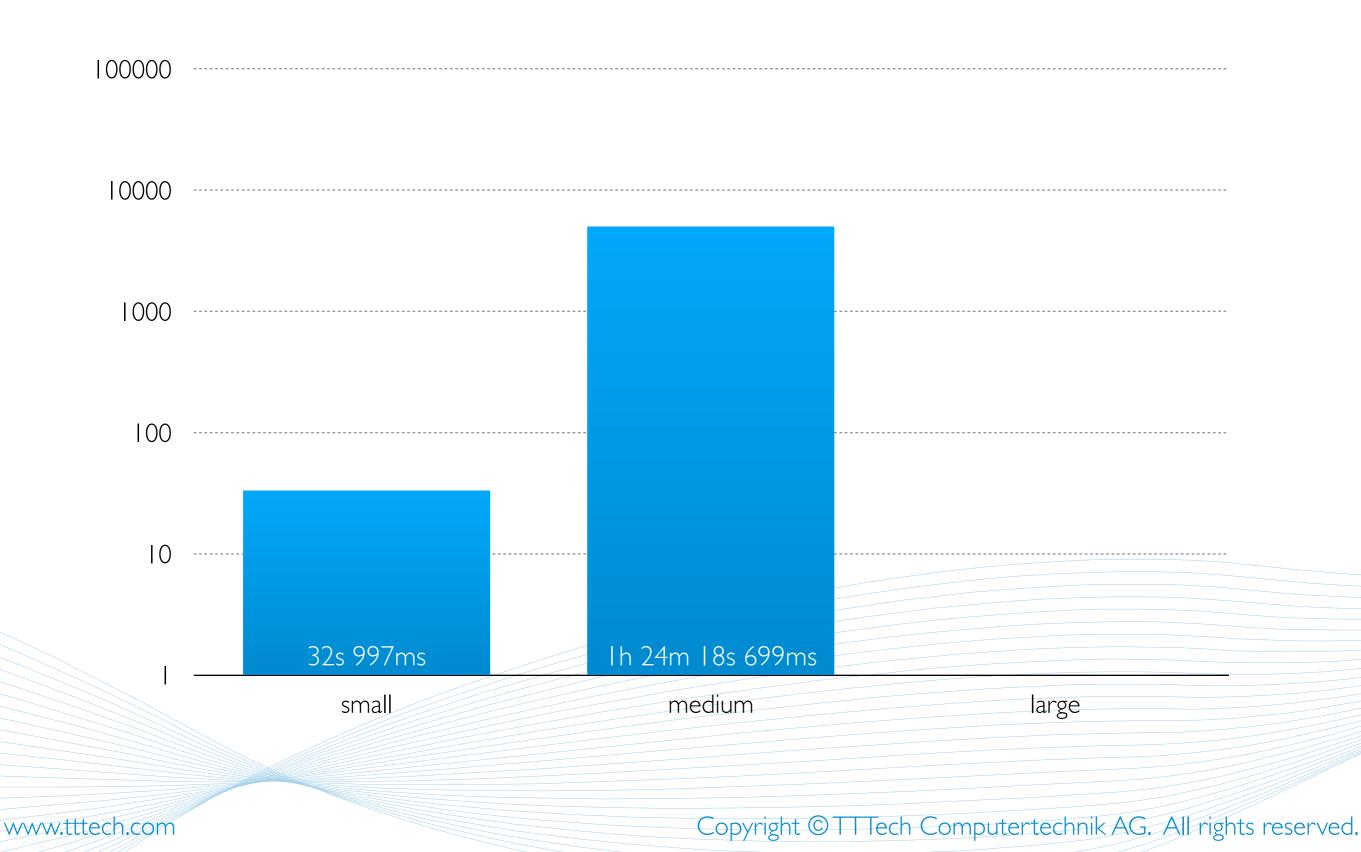


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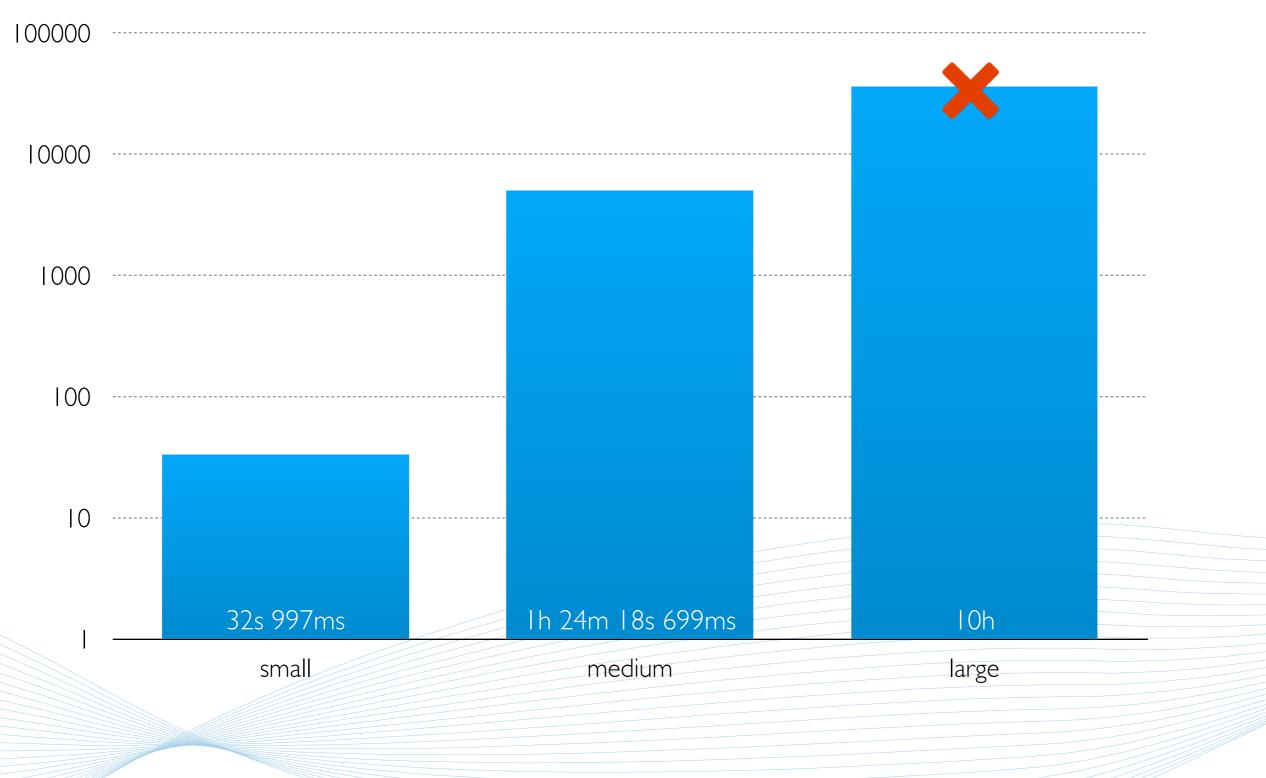


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where does the complexity come from?

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where does the complexity come from?

where do the frames come from?



where does the complexity come from?

where do the frames come from?

consumer tasks producer tasks communication





where does the complexity come from?

where do the frames come from?

consumer tasks producer tasks communication









where does the complexity come from?

where do the frames come from?

consumer tasks producer tasks communication

free tasks





where does the complexity come from?

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consumer tasks producer tasks communication

free tasks



#### let's treat them differently

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#### Demand-based



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free tasks





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SMT

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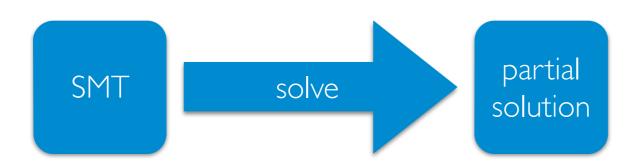
free tasks





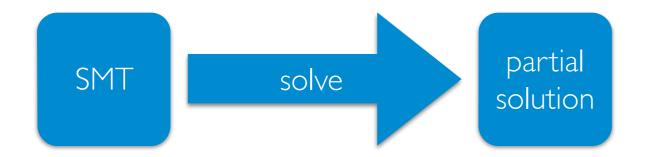


free tasks



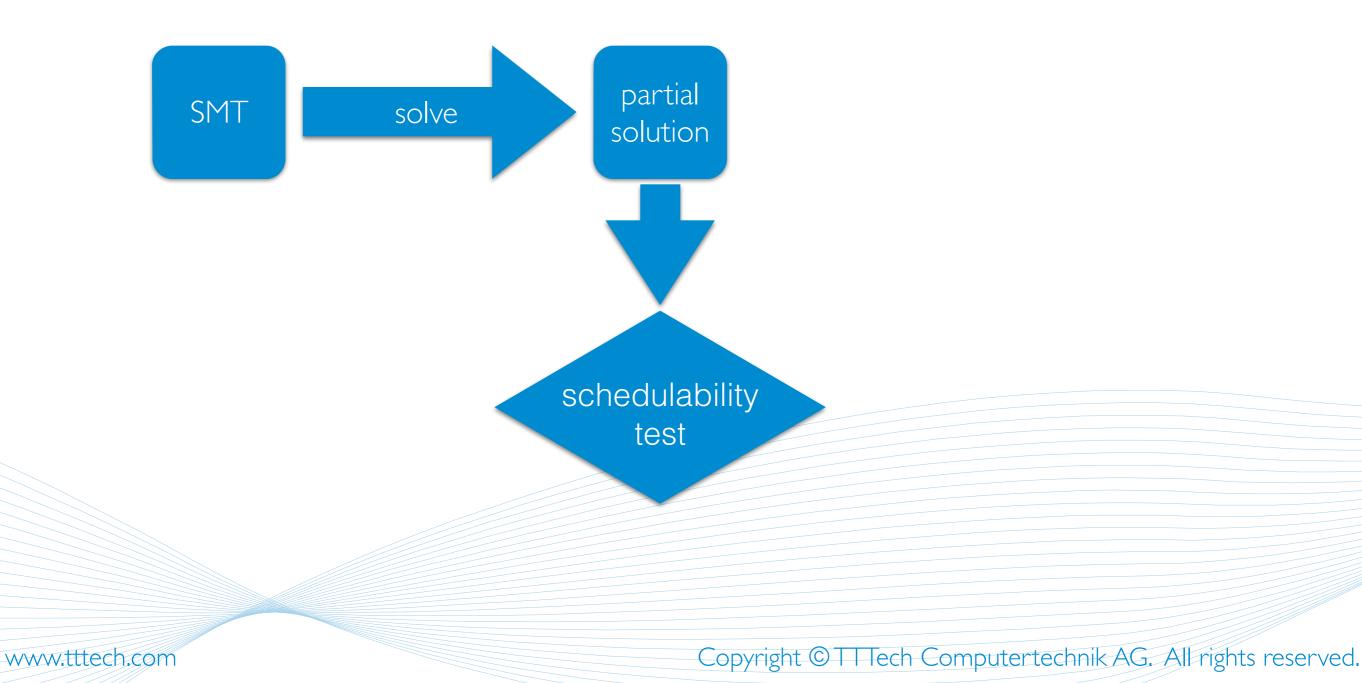




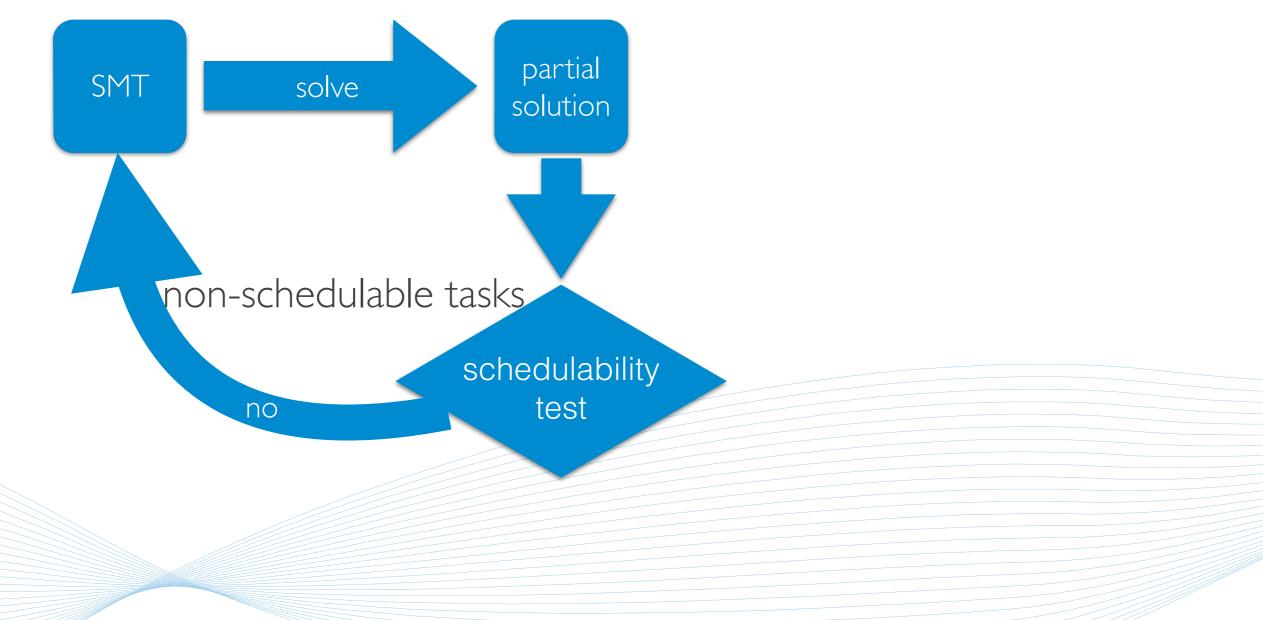


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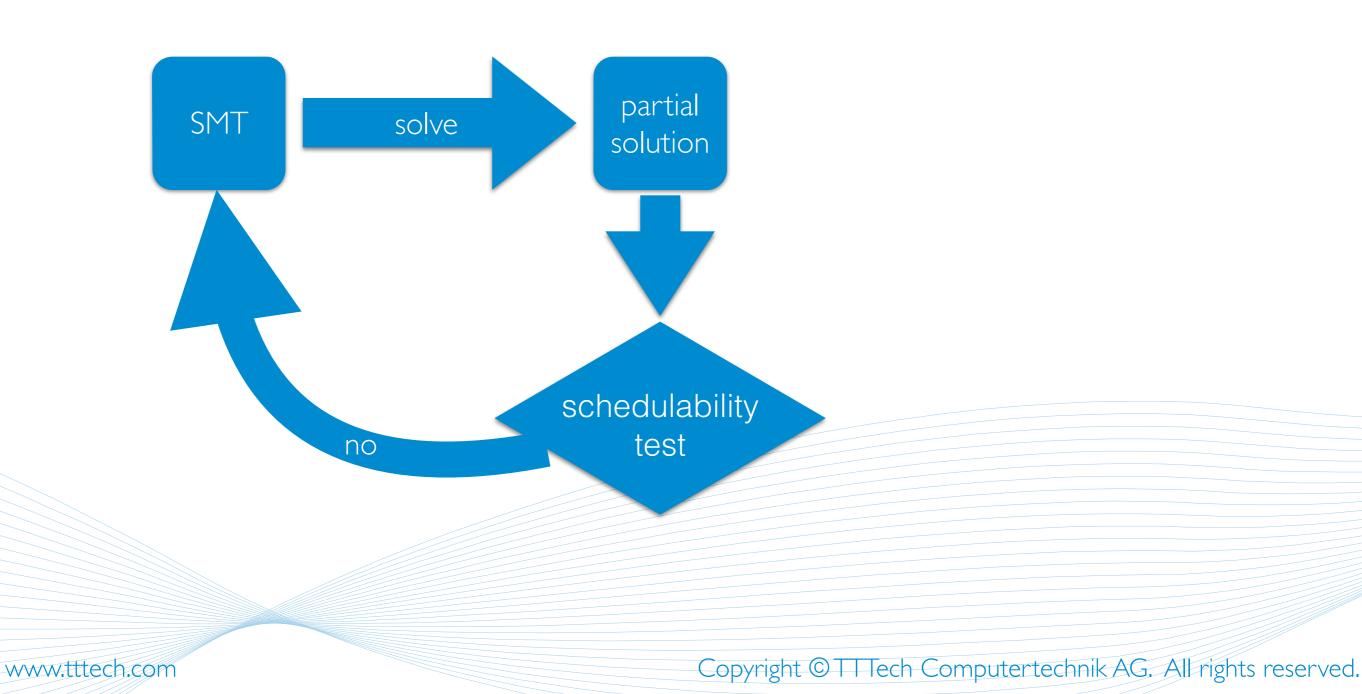




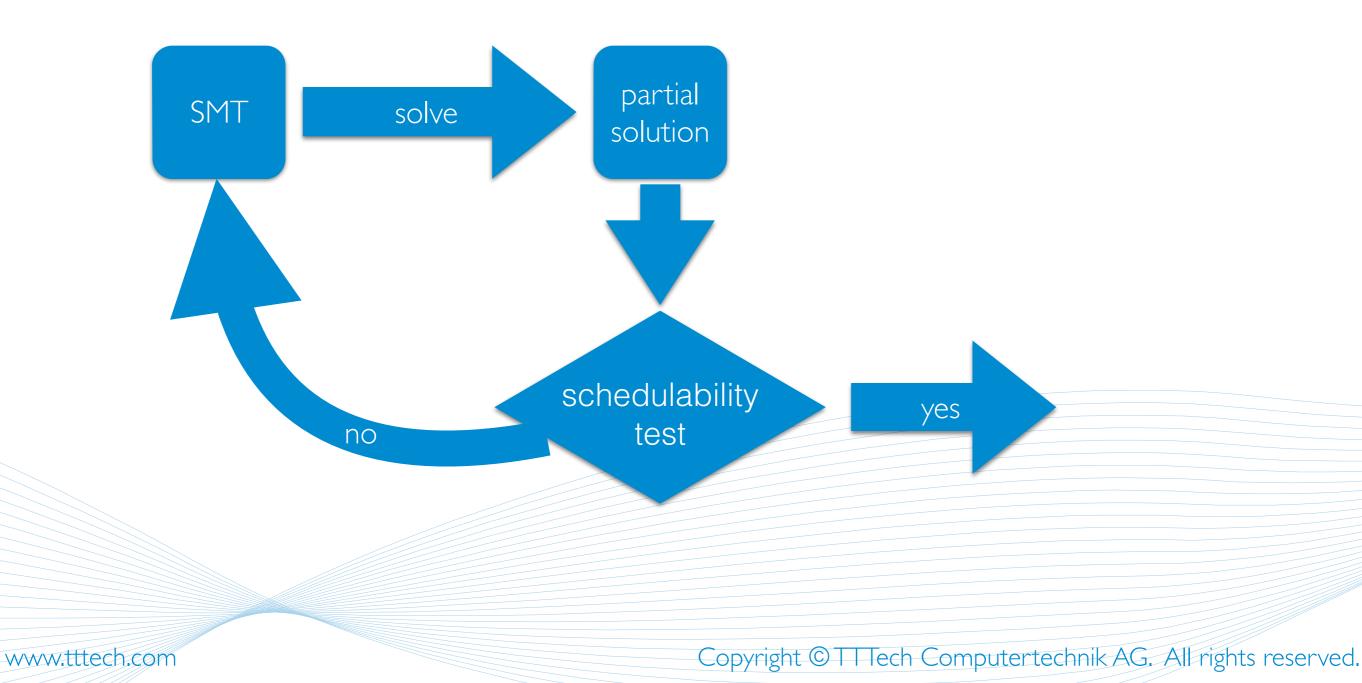


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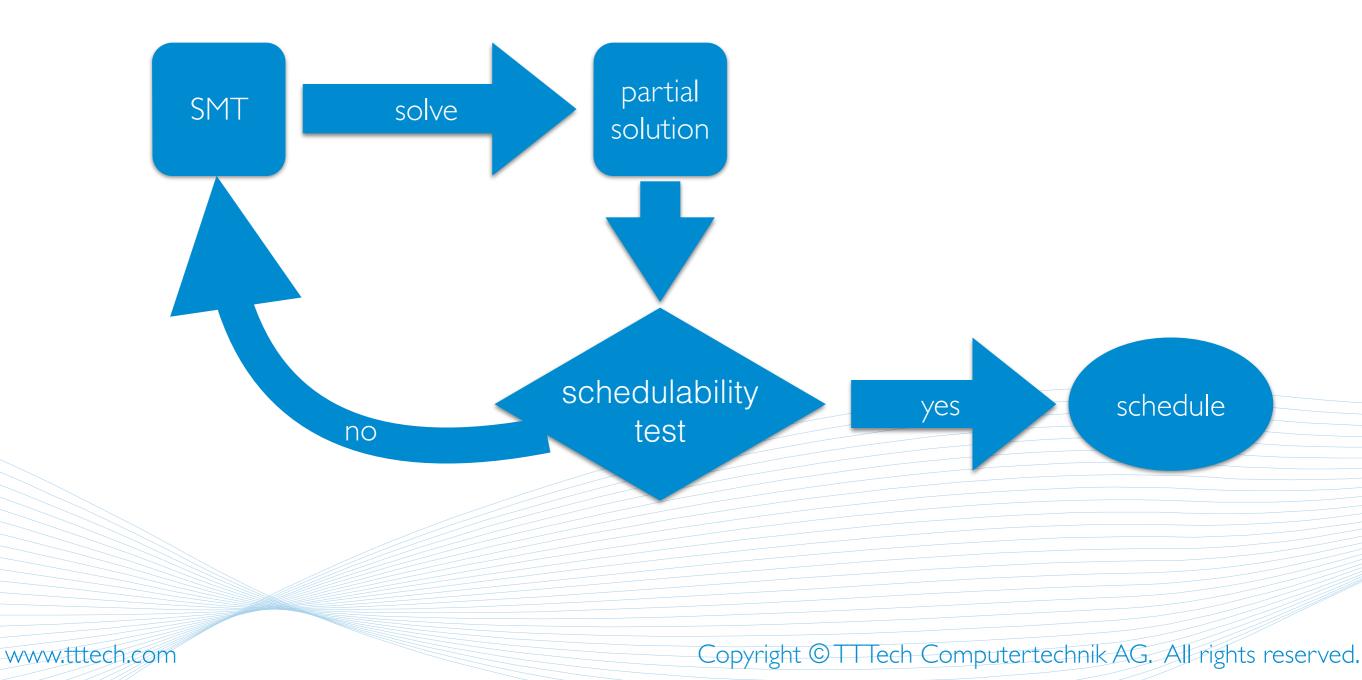








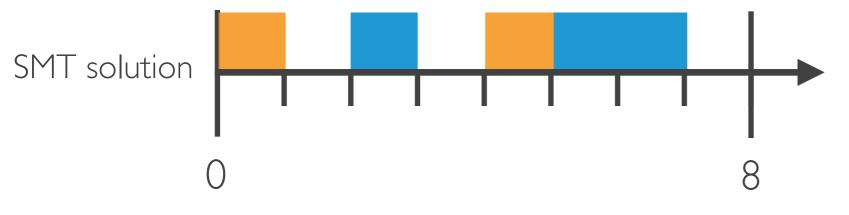




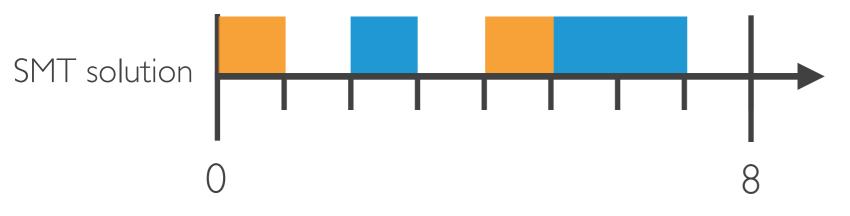


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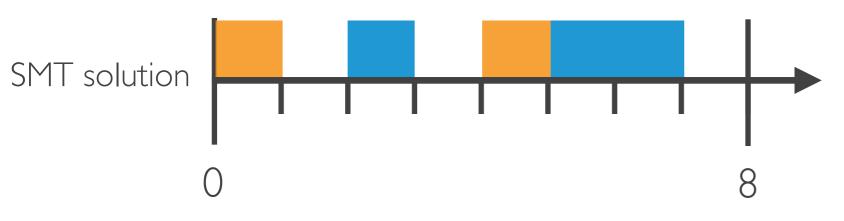






#### EDF tasks

	(0,  , 8,  )
	(2,  , 8,  )
	(4,  , 8,  )
	(5, 2, 8, 2)



#### EDF tasks

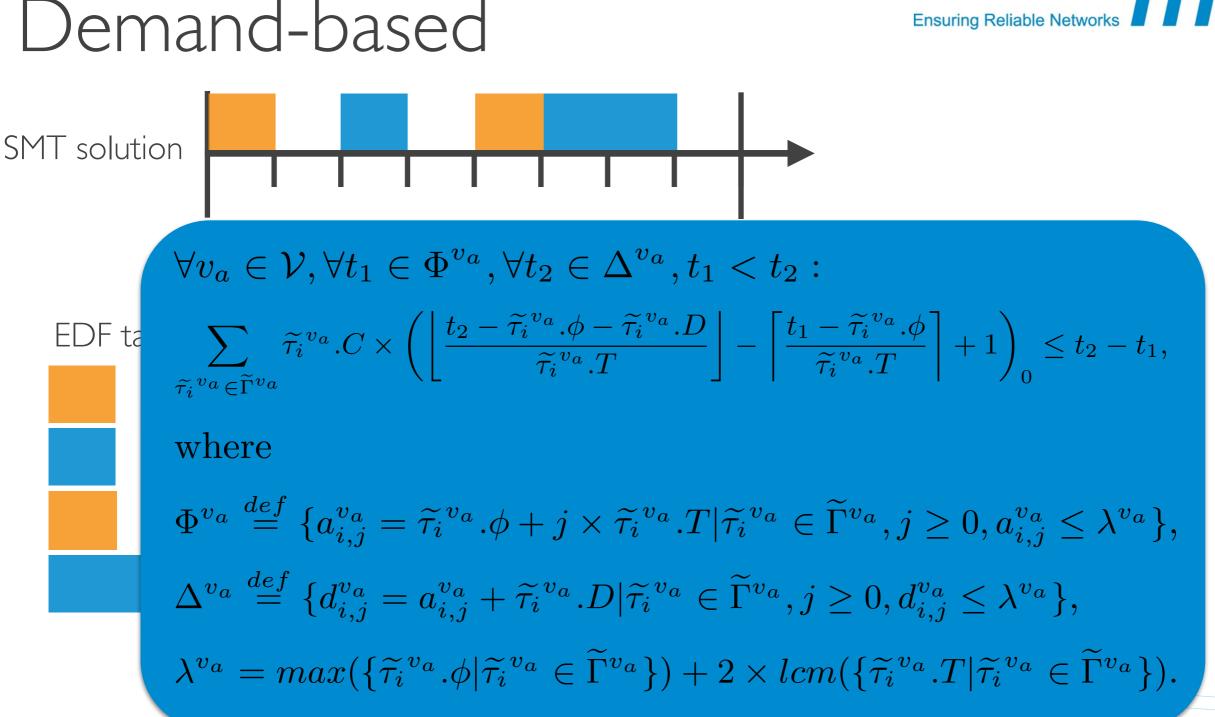


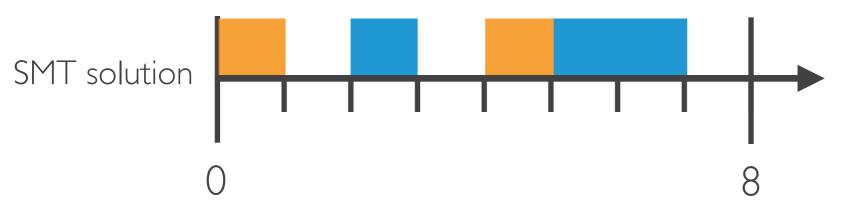
#### free tasks





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#### EDF tasks



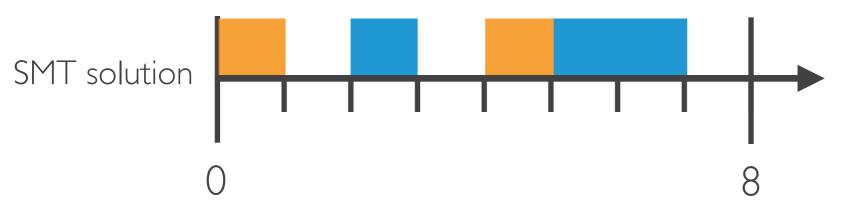
#### free tasks



# $$\begin{split} \forall v_a \in \mathcal{V}, \forall t_1 \in \Phi^{v_a}, \forall t_2 \in \Delta^{v_a}, t_1 < t_2: \\ \sum_{\tilde{\tau_i}^{v_a} \in \tilde{\Gamma}^{v_a}} \tilde{\tau_i}^{v_a}.C \times \left( \left\lfloor \frac{t_2 - \tilde{\tau_i}^{v_a}.\phi - \tilde{\tau_i}^{v_a}.D}{\tilde{\tau_i}^{v_a}.T} \right\rfloor - \left\lceil \frac{t_1 - \tilde{\tau_i}^{v_a}.\phi}{\tilde{\tau_i}^{v_a}.T} \right\rceil + 1 \right)_0 \leq t_2 - t_1, \\ \text{where} \\ \Phi^{v_a} \stackrel{def}{=} \left\{ a_{i,j}^{v_a} = \tilde{\tau_i}^{v_a}.\phi + j \times \tilde{\tau_i}^{v_a}.T | \tilde{\tau_i}^{v_a} \in \tilde{\Gamma}^{v_a}, j \geq 0, a_{i,j}^{v_a} \leq \lambda^{v_a} \right\}, \\ \Delta^{v_a} \stackrel{def}{=} \left\{ d_{i,j}^{v_a} = a_{i,j}^{v_a} + \tilde{\tau_i}^{v_a}.D | \tilde{\tau_i}^{v_a} \in \tilde{\Gamma}^{v_a}, j \geq 0, d_{i,j}^{v_a} \leq \lambda^{v_a} \right\}, \\ \lambda^{v_a} = max(\{\tilde{\tau_i}^{v_a}.\phi|\tilde{\tau_i}^{v_a} \in \tilde{\Gamma}^{v_a}\}) + 2 \times lcm(\{\tilde{\tau_i}^{v_a}.T|\tilde{\tau_i}^{v_a} \in \tilde{\Gamma}^{v_a}\}). \end{split}$$

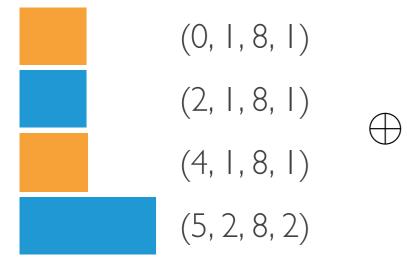
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#### EDF tasks

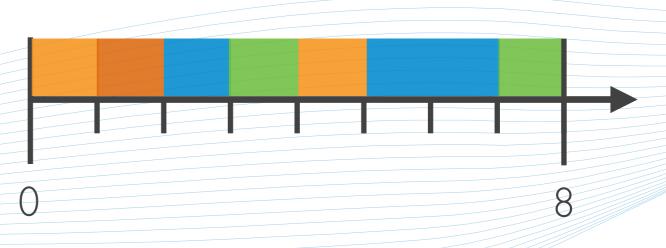
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#### free tasks

	(0,	2,	8,	8)
	(0,	Ι,	8,	8)

# $$\begin{split} \forall v_a \in \mathcal{V}, \forall t_1 \in \Phi^{v_a}, \forall t_2 \in \Delta^{v_a}, t_1 < t_2: \\ \sum_{\tilde{\tau_i}^{v_a} \in \tilde{\Gamma}^{v_a}} \tilde{\tau_i}^{v_a}.C \times \left( \left\lfloor \frac{t_2 - \tilde{\tau_i}^{v_a}.\phi - \tilde{\tau_i}^{v_a}.D}{\tilde{\tau_i}^{v_a}.T} \right\rfloor - \left\lceil \frac{t_1 - \tilde{\tau_i}^{v_a}.\phi}{\tilde{\tau_i}^{v_a}.T} \right\rceil + 1 \right)_0 \leq t_2 - t_1, \\ \end{split}$$ where $\Phi^{v_a} \stackrel{def}{=} \{a_{i,j}^{v_a} = \tilde{\tau_i}^{v_a}.\phi + j \times \tilde{\tau_i}^{v_a}.T | \tilde{\tau_i}^{v_a} \in \tilde{\Gamma}^{v_a}, j \geq 0, a_{i,j}^{v_a} \leq \lambda^{v_a} \}, \\ \Delta^{v_a} \stackrel{def}{=} \{d_{i,j}^{v_a} = a_{i,j}^{v_a} + \tilde{\tau_i}^{v_a}.D | \tilde{\tau_i}^{v_a} \in \tilde{\Gamma}^{v_a}, j \geq 0, d_{i,j}^{v_a} \leq \lambda^{v_a} \}, \\ \lambda^{v_a} = max(\{\tilde{\tau_i}^{v_a}.\phi|\tilde{\tau_i}^{v_a} \in \tilde{\Gamma}^{v_a}\}) + 2 \times lcm(\{\tilde{\tau_i}^{v_a}.T|\tilde{\tau_i}^{v_a} \in \tilde{\Gamma}^{v_a}\}). \end{split}$







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• transform scheduled frames on CPUs into asynchronous periodic tasks



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- add free tasks and apply schedulability test [Pellizzoni@RealTimeSyst05]



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- incremental algorithm so we don't lose schedulability
- we are still exponential but scale better for the average case

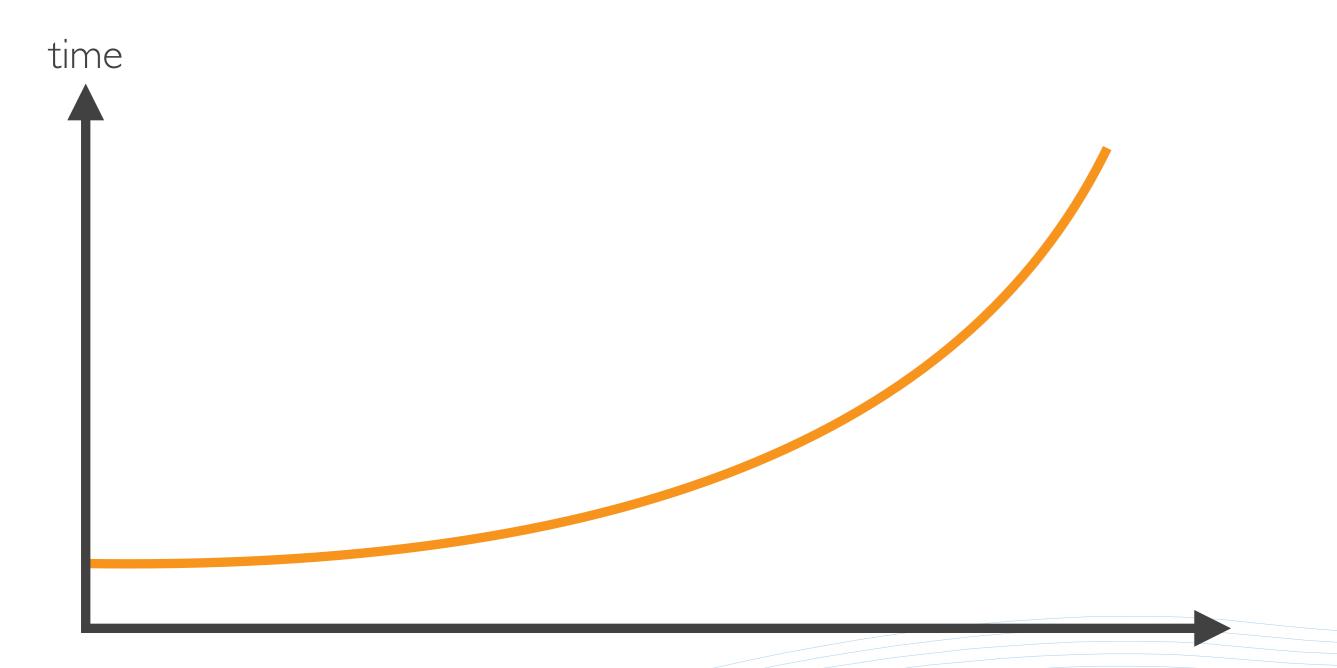


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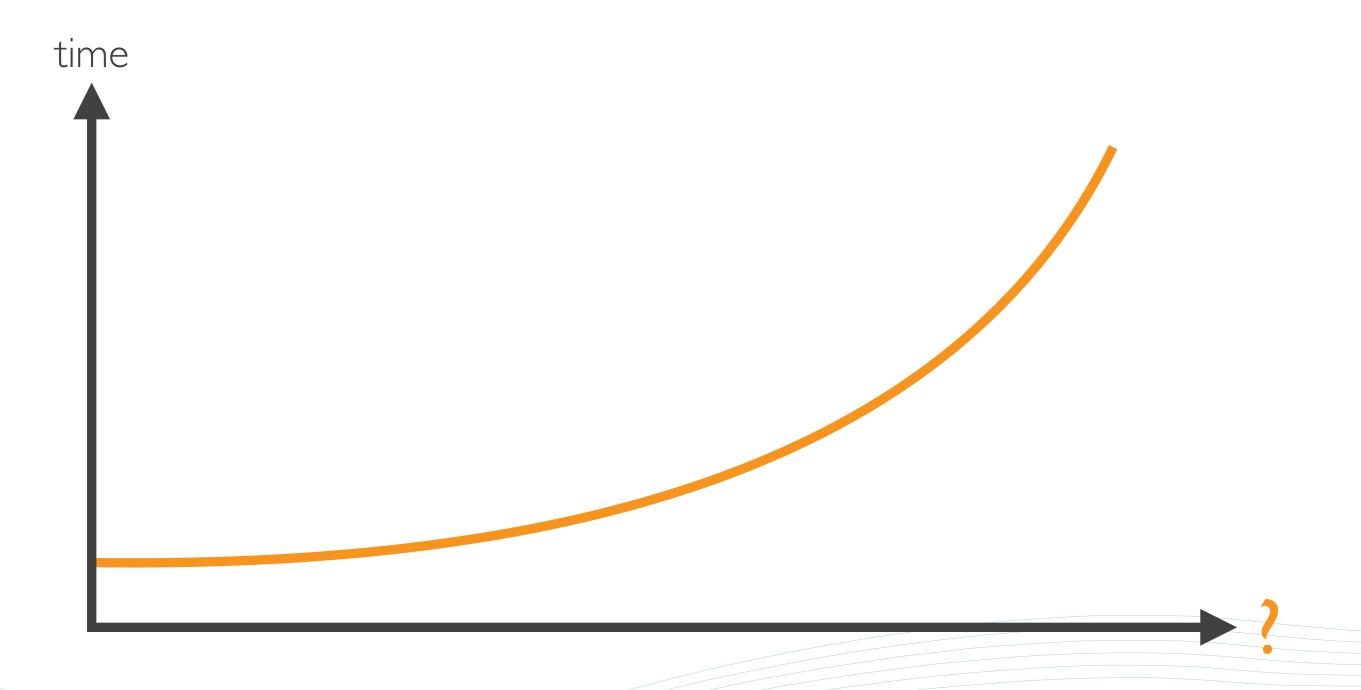




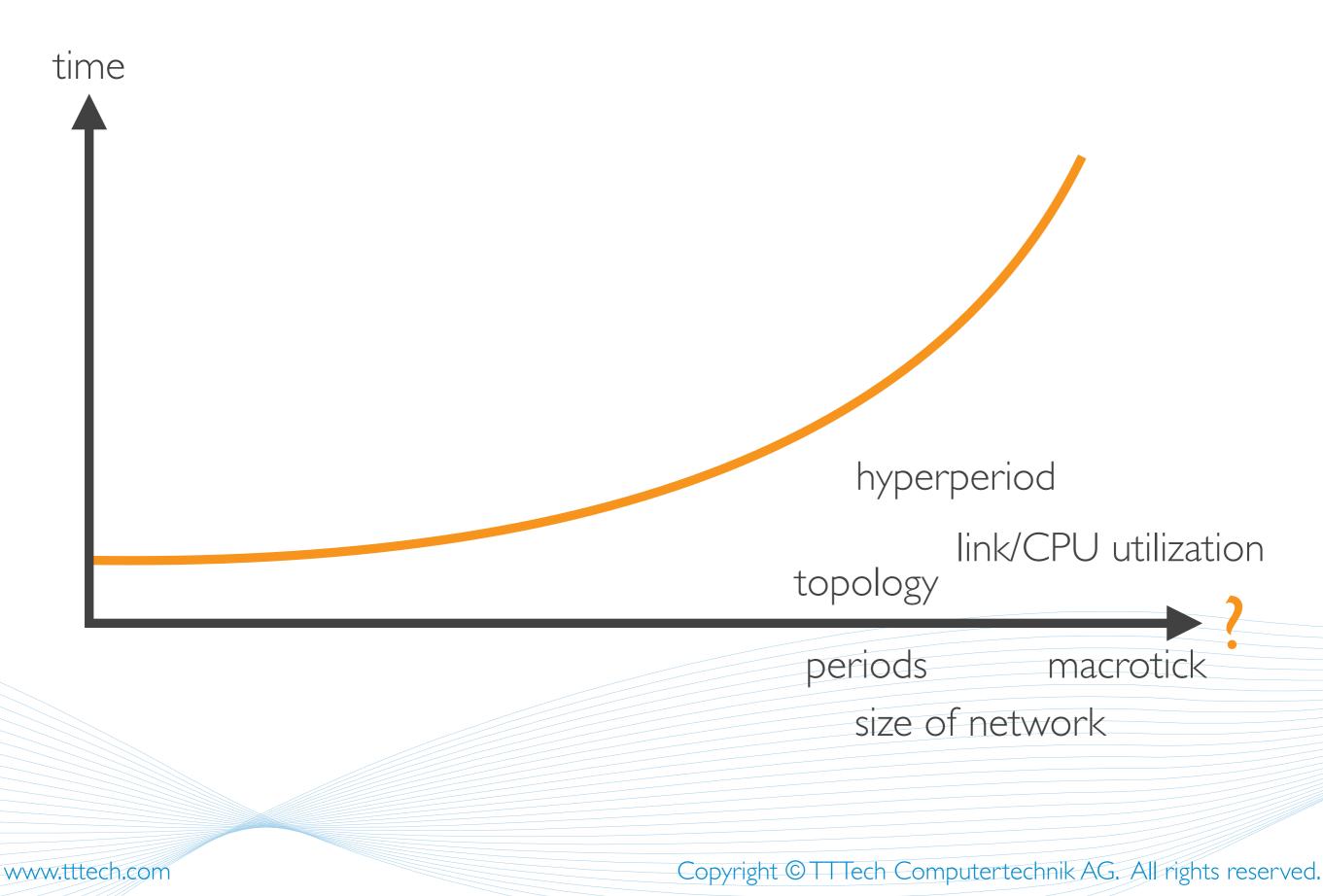


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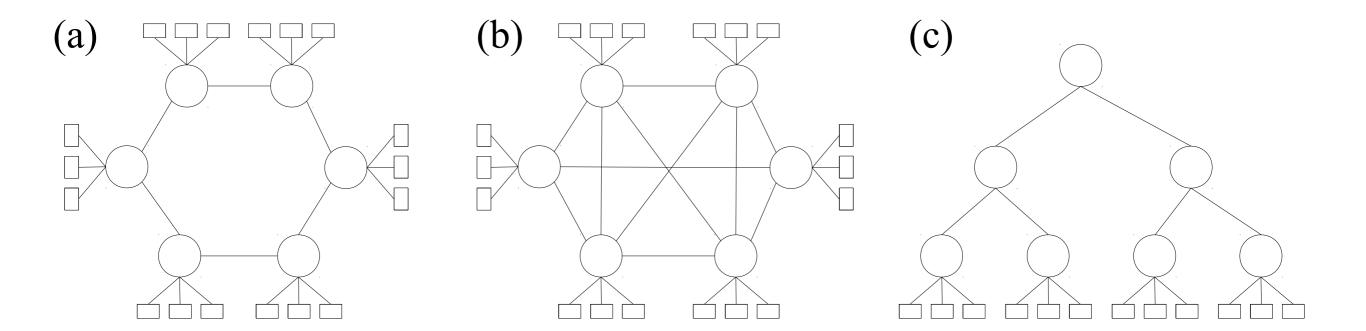








### Topologies



Periods { | 0,20,25,50, | 00}, { | 0,30, | 00}, {50,75} ms

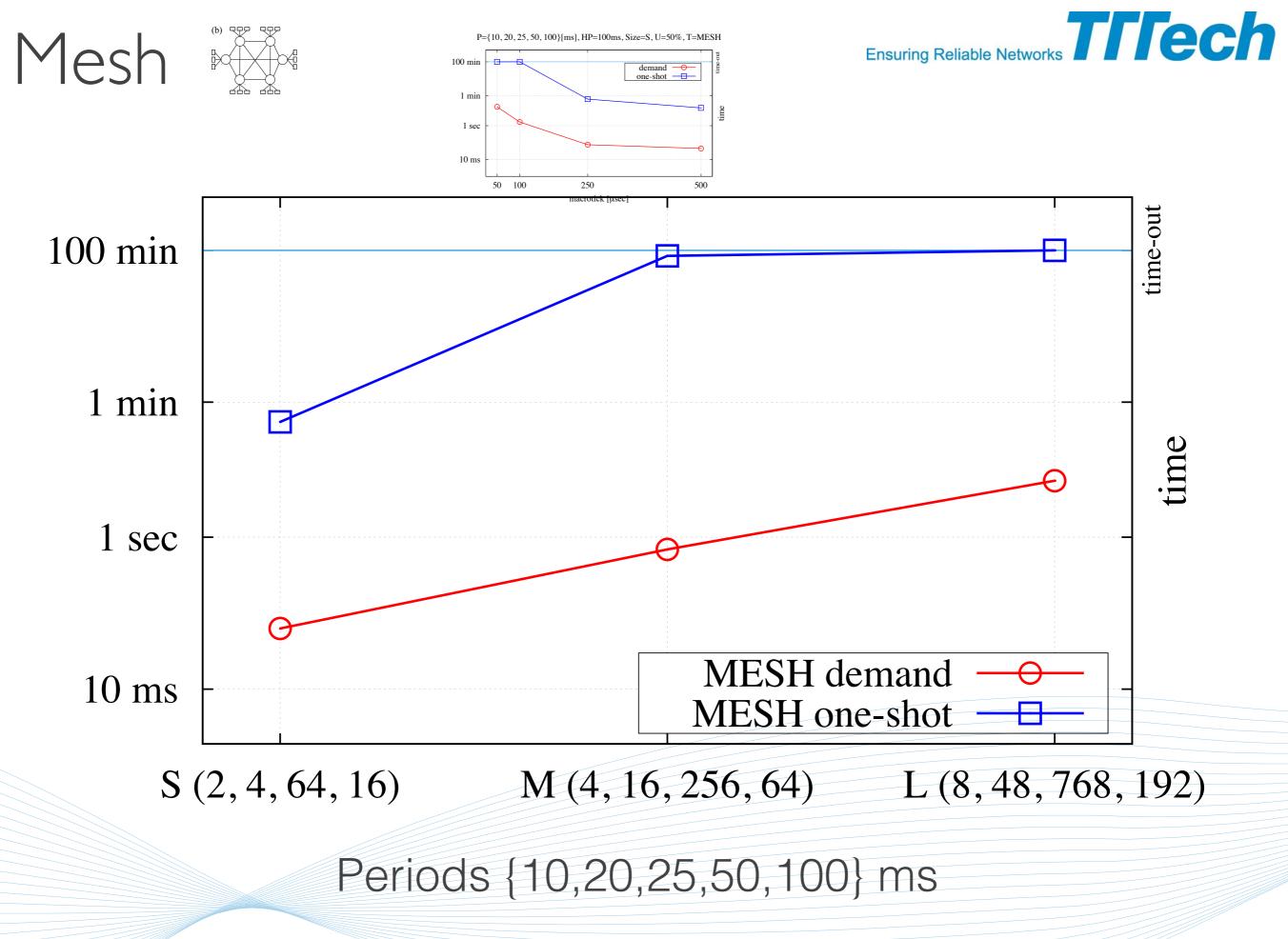
l usec network link granularity

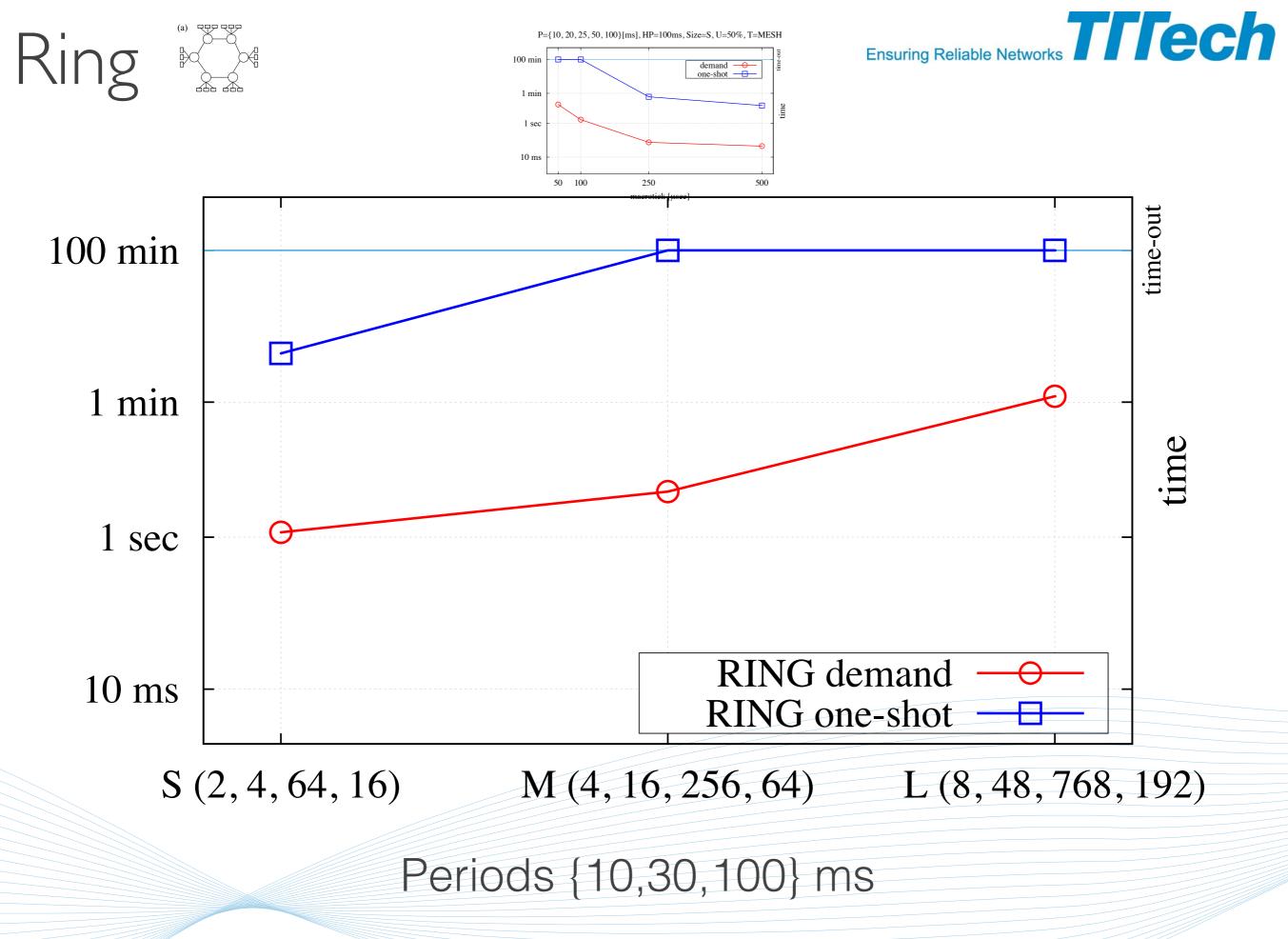
100Mbit/s and 1Gbit/s

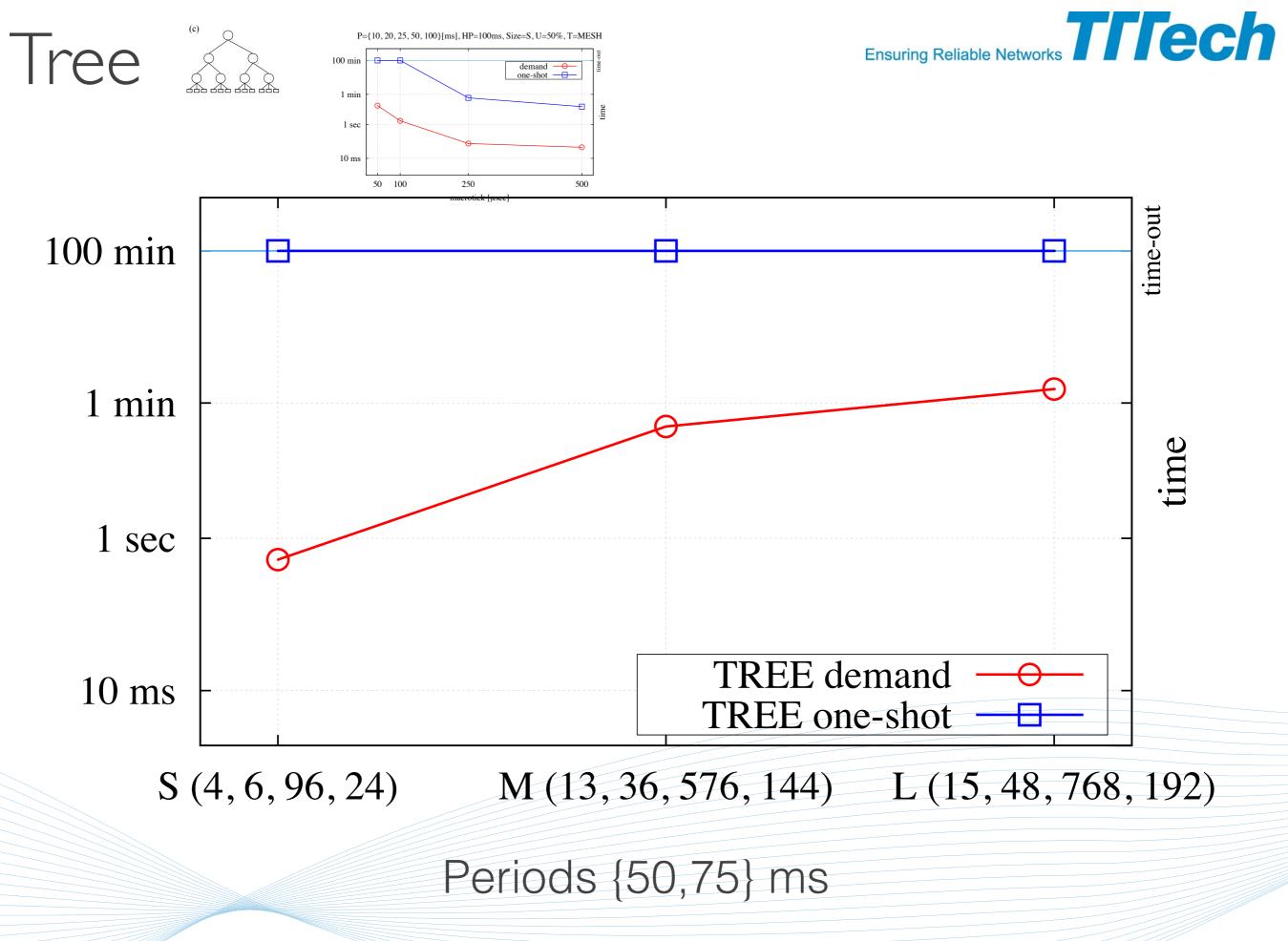
random message size and virtual links

different macrotick and utilization configurations

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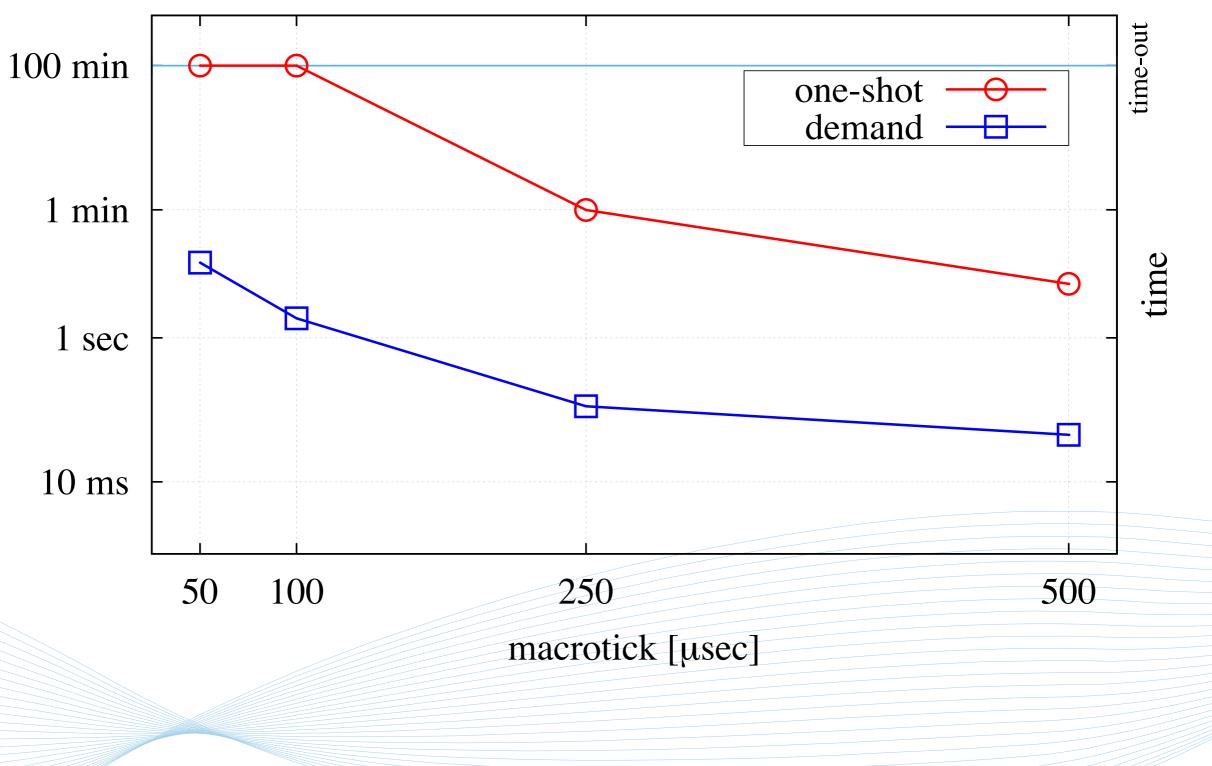




#### Macrotick

Ensuring Reliable Networks

P={10, 20, 25, 50, 100}[ms], HP=100ms, Size=S, U=50%, T=MESH

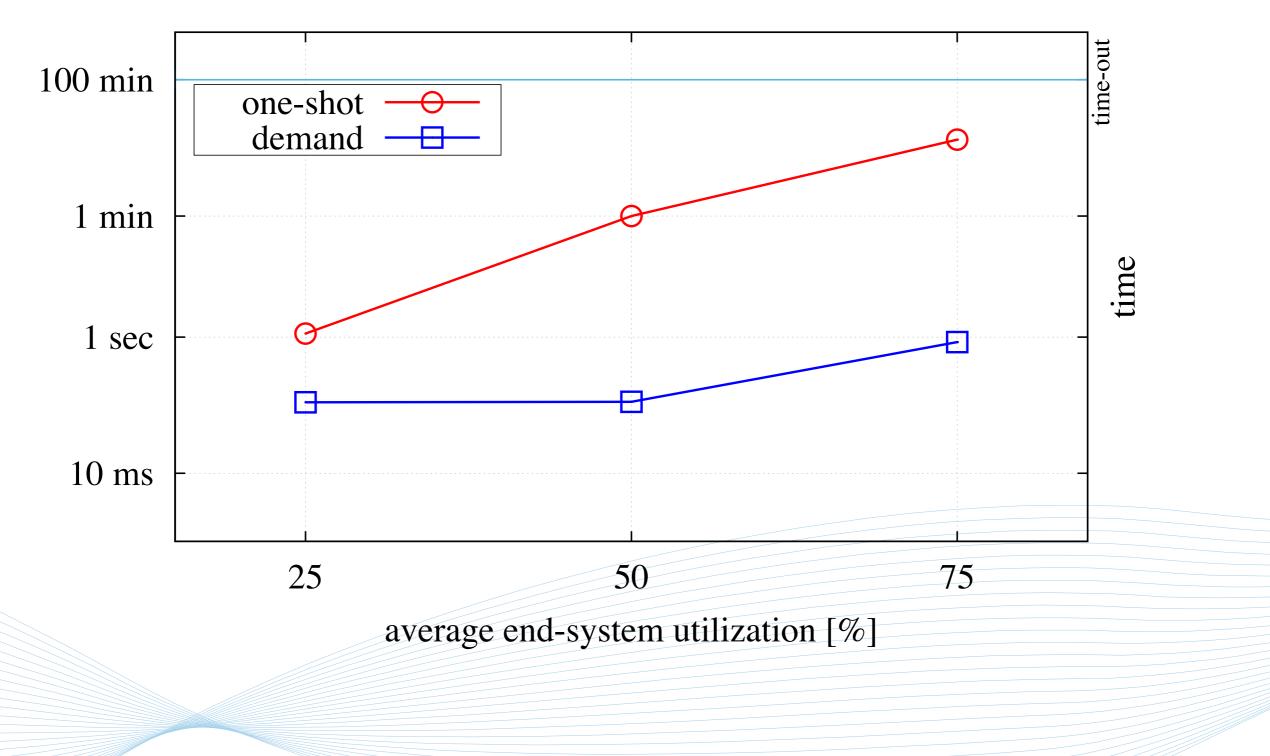


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#### Utilization

Ensuring Reliable Networks

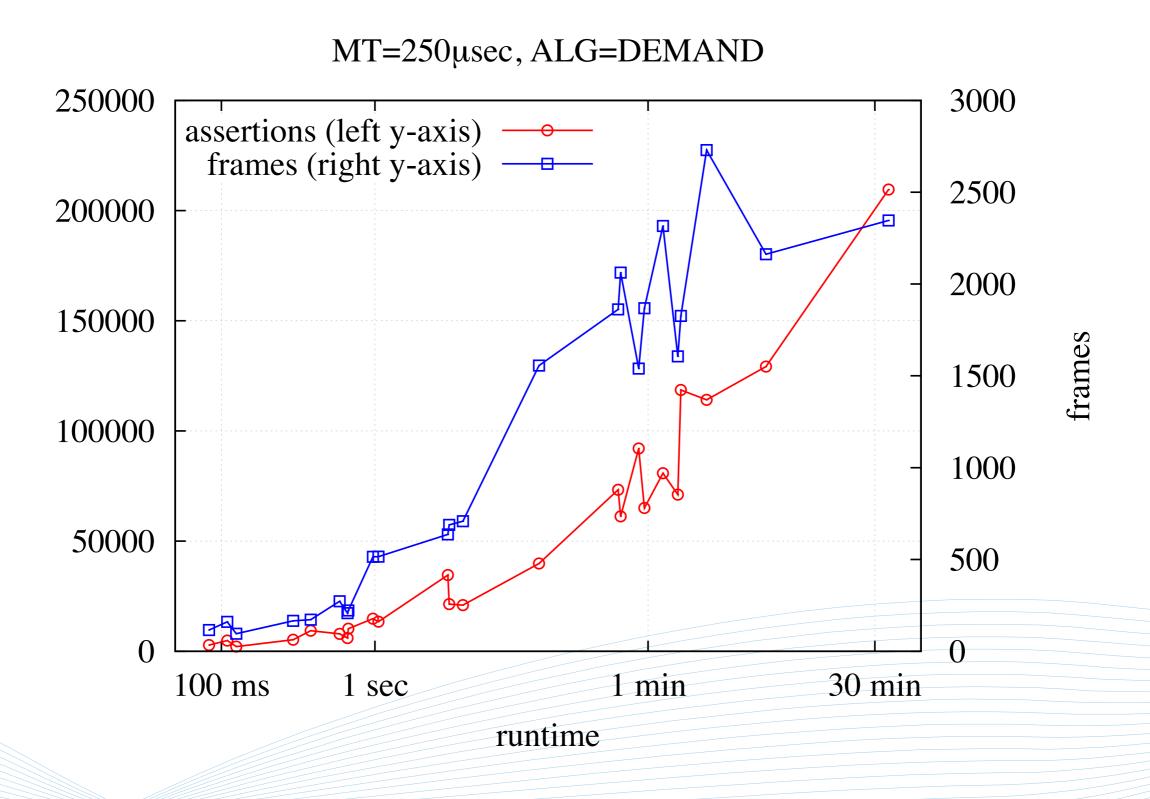
P={10, 20, 25, 50, 100}[ms], HP=100ms, MT=250µsec, Size=S, T=MESH



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### SMT assertions





assertions



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#### co-synthesis of task and message schedules

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co-synthesis of task and message schedules preemptive tasks





- co-synthesis of task and message schedules preemptive tasks
- switched multi-speed TTEthernet networks





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- co-synthesis of task and message schedules
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- scales for medium to large industrial systems



### Thank you!

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### SMT-scheduled frames

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