



Antinomy between Schedulability and Quality of Control using a Feedback Scheduler **RTNS'2014**

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- Introduction
- Antinomy in co-design
- Scheduling artifacts characterization
- Conclusion



Traditional real-time scheduling models give poor support for scheduling/control co-design...

Antinomy in codesign...

Off-line optimization





RM scheduled periodic tasks with implicit deadlines



The feedback scheduler





[Liu & Layland '73]

$$\sum U_i \leq n \left(2^n - 1\right)$$

[Bini '03] (hyperbolic condition)

$\prod (U_i + 1) \leq 2$

CIAS Timings and delays



Sampling latency: higher priority task execution

I/O latency: execution time + higher priority preemption

Scheduling artifacts: latencies and jitters...

Antinomy in codesign...



- Three servo-motors with a PID regulator
 - Well known study case from [Åström & Hägglund]
 - Adaptive samples: backward difference for derivative
 - Controlled by a single processor computer
- Three inverted pendulums with cart
 - Another well studied benchmark [Åström & Furuta]
 - Strongly non linear three order coupled system
 - With cart: only horizontal moves

Antinomy in codesign...

CIAS Three servo-motors example



- Controller performance parameters: $(\omega_{0,}\xi)=(20, 0.707)$
- Use of adaptive samples in the PID

Antinomy in codesign...

Simulation setup





Minimizing tasks' period improves quality of control...

Performance analysis

- Three periodic tasks: nominal period $h_i^{nom} \rightarrow task$ priority (RM)
- Feedback scheduling: $h_i^{k+1} = \alpha h_i^k \rightarrow reach the utilization bound$
- Execution time: $3 \le Ci \le 5$ ms (Weibull distribution)

Bound	L&L test (U < 0.69)			Hyperbolic test			Threshold (U = 0.5)		
h	τ,	τ2	τ ₃	τ ₁	τ2	τ ₃	τ,	τ2	τ ₃
Error	0.063	0.065	0.64	0.060	0.062	1.35	0.088	768.7	>108
Sampling period (ms)	12.52	15.55	18.79	12.40	15.51	18.60	19.43	24.24	29.15
I/O latency (ms)	3.88	5.24	7.32	3.88	5.09	7.93	3.87	4.84	5.28



Scheduling artifacts (response time and jitter) increase when processor utilization increases (controller tasks periods decrease).

The degradation caused by these phenomena on a PID controller can be greater than the gain generated by the increase in sampling rate.



- Three servo-motors: periodic tasks τ_1 , τ_2 , τ_3
- Scheduled with RM (tie breaker: smallest task index)

	C _i	h _i ^{nom}		
\mathbf{T}_{1}	8.85	17.7		
τ ₂	8.85	17.7		
τ ₃	8.85	17.7		



Antinomy in codesign...

IAS / The antinomy illustrated





Artifact characterization

• Three servo-motors example

							100-
	C ,	h _i ^{nom}	Mode	k	μ	λ	50- <i>∞</i> [°]
τ ₁		6	3.2	3.1	0.2	3	
τ ₂	3.4	13	3.2	3.1	0.2	3	0
T ₃		14	3.2	3.1	0.2	3	Error cost function of
							mean sample periods
							for task ${f \tau}_{_3}$

Artifact characterization



Error cost function of IO and sampling latencies for \mathbf{T}_{3}

Linear correlation (SRS): 0.95 (I/O) and -0.81 (Samp)

Error cost function of control jitter for \mathbf{T}_{3}

Linear correlation (SRS): -0.88

Antinomy in codesign...

Artifact characterization

• Three inverted pendulum example



Conclusion & perspectives

- Do not (always) trust intuitive assumptions
- Impact of scheduling artifacts on QoC
 - Try to keep I/O latency low...
- Contribution
 - Identify scheduling parameters that deteriorate a real-time control when the lower priority task's frequency tends toward the closed-loop system bandwidth
- Perspective: guidelines for better co-design...



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Thank you for your attention