Real-time Ethernet Residual Bus Simulation: A Model-Based Testing Approach for the Next-Generation In-Car Network

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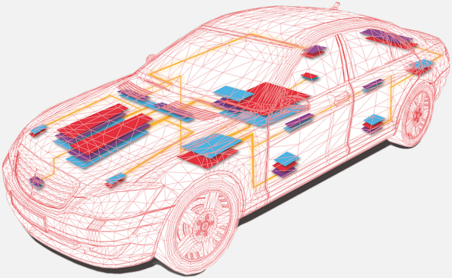
Software and functions in modern cars



- Functions are implemented mostly in software today
- Utilization of software directly influences the development costs
- Testing in early development stages reduces these costs
- Distributed development makes early testing difficult

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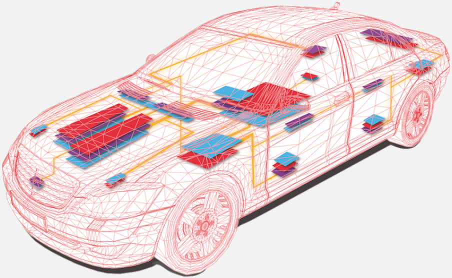

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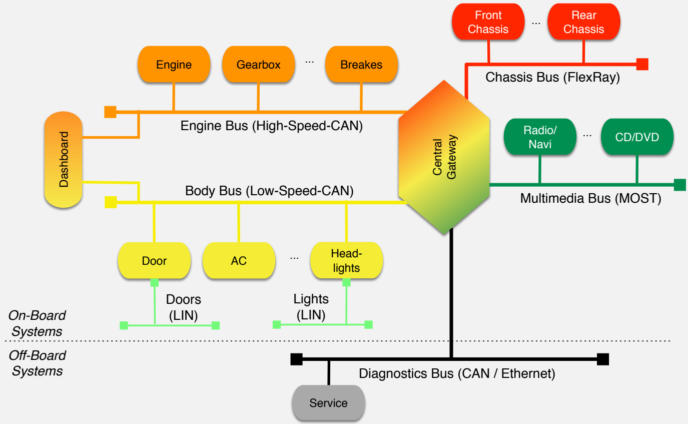
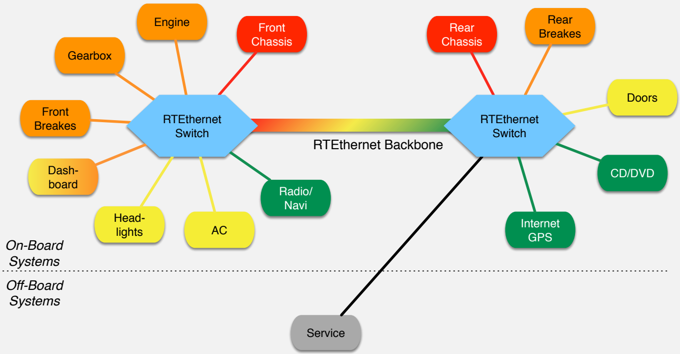
Complex In-Car Interconnections



- The complexity of current in-car interconnections is hardly manageable

Complex In-Car Interconnections



- RT Ethernet for in-car interconnection reduces the complexity

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Contribution

- Testing systems and applications in early development stages is important
- New applications will rely on RT Ethernet as communication technology
- Suitable methodology is needed to validate distributed applications

- RT Ethernet *Residual Bus Simulation* enables early testing
- Combination of model-based testing principles to validate non-functional requirements

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Agenda

Model-based Testing Approach

- The automotive development process is model driven
- Models are utilized as specifications for
  - Representing implementation details
  - Modeling system requirements
- Test cases are systematically inherited from models
- Execution of cases on different test platforms
  - MiL, SiL, PiL, HiL and *Residual Bus Simulation*

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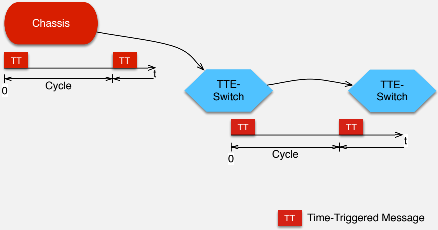
Residual Bus Simulation

- The remaining network is simulated from the viewpoint of the SUT
- SUT and simulator are coupled via the communication interface
- Behavior and network specific characteristics are realistically emulated
- The simulator pretends to be a physical system

- TTEthernet provides three different message classes



- Static designed routing for deterministic behavior
- Synchronized time base for time-triggered communication

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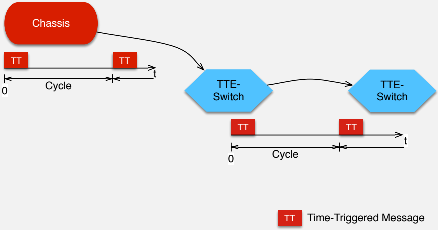

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RT Ethernet as In-Car Network

Attributes of TTEthernet

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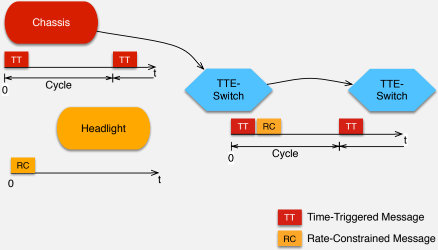

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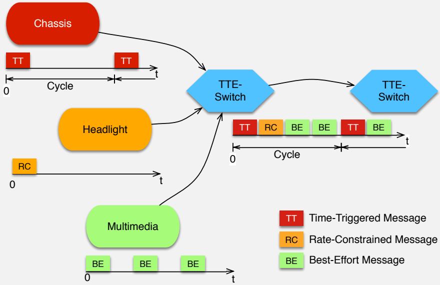

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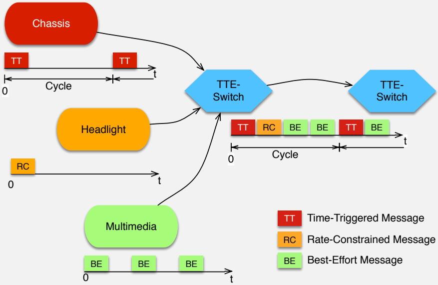

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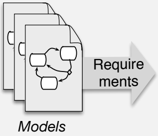
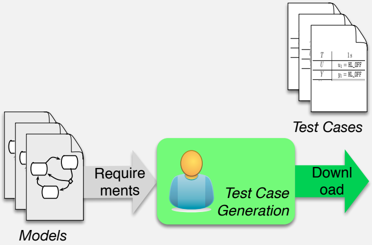
Model-based Methodology

Overview



- Requirements are modeled within suitable diagrams
- Test cases are inherited from the diagrams
- Test cases are executed on a suitable residual bus simulation platform



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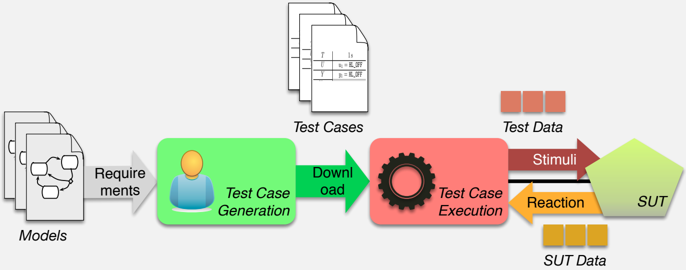

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Modeling System Requirements
UML-MARTE

- Classic UML is not sufficient for embedded Real-time Systems
- Utilization of UML-Profile *Modeling and Analysis of Real-time Embedded Systems (MARTE)*

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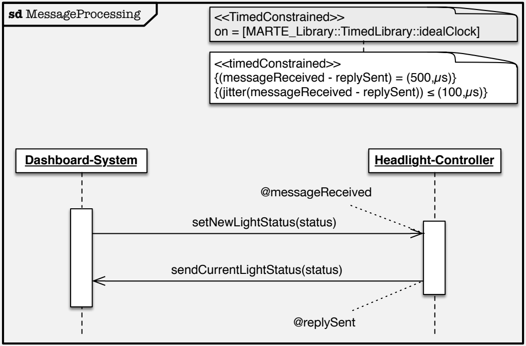
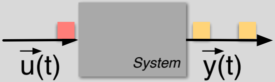


Base Model



- $ATC_{FR} = (T, U, Y)$
- Modeling specific values of inputs and outputs at specific points in time

Extending the Model

- $ATC_{NFR} = (T, U, Y, L, R, \Delta_L, \Delta_R)$
- Extending with reply time (*latency*) & transmission rate (*rate*)

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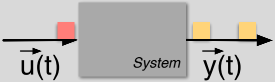

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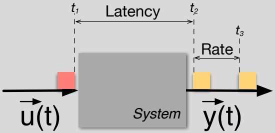

- $ATC_{NFR} = (T, U, Y, L, R, \Delta_L, \Delta_R)$
- Extending with reply time (*latency*) & transmission rate (*rate*)

- Abstract representation of to be generated test data
- Modeling functional requirements with expected output
- Modeling non-functional requirements with expected timing constraints
- Utilization as simulation model to drive the simulator

Requirements

- TTEthernet compliant message transmission
- Support of timing analyzes
- Execution of the abstract test case model

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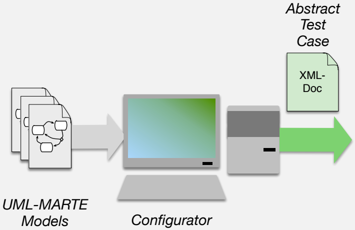

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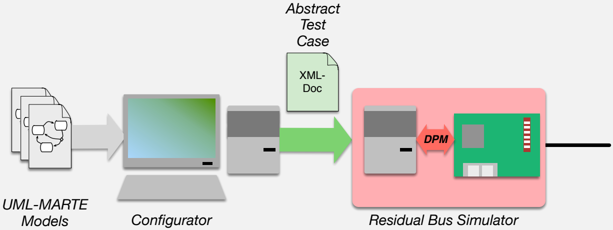

Implementation of our Approach

Requirements and Architecture

Requirements

- TTEthernet compliant message transmission
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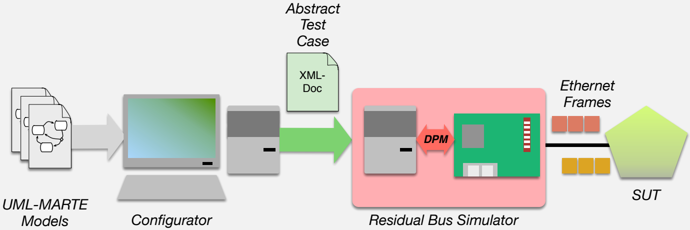

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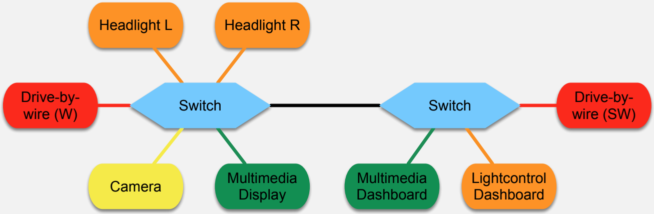
Overview of the physical system



- Light control dashboard transmits new light states
- Headlights reply each received light state and
- Periodically provide their current light state
- Light control dashboard presents the light state to the user

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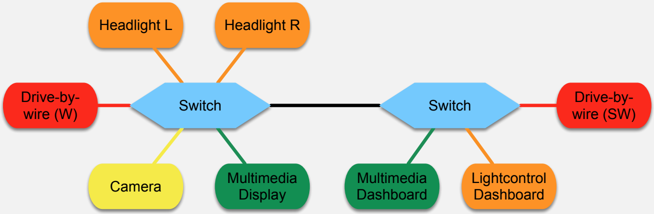

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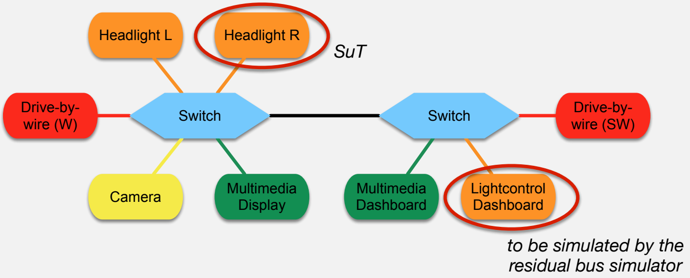

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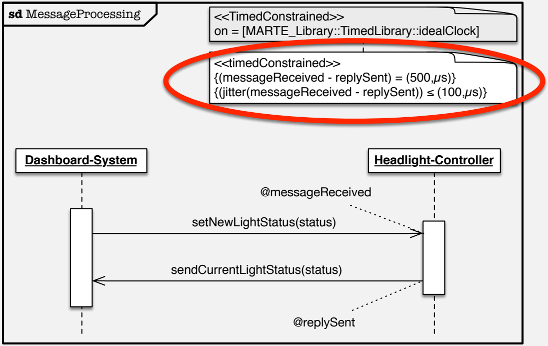
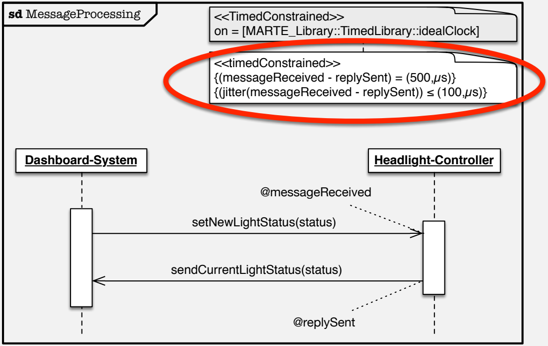


- Timing requirements of the reply message
  - Latency: 500 μs
  - Jitter: ± 50 μs



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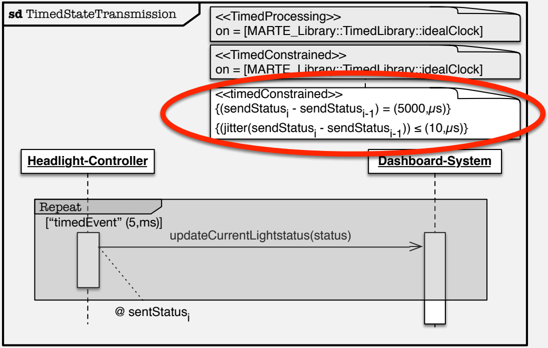
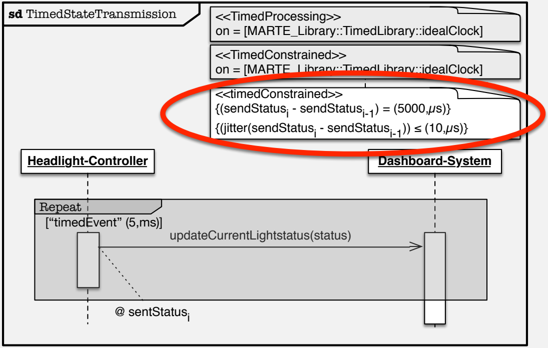


- Timing requirements of the message transmission
  - Rate: 5000 µs
  - Jitter: ± 5 µs

Validating the Headlight Controller

Requirement Modelling with UML-MARTE



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Validating the Headlight Controller

T	1 s	2 s	5 s	7 s	9 s	11 s
U	u_1 = HL_OFF	u_1 = LED_0	u_1 = LED_100	u_1 = LED_50	u_1 = LED_101	u_1 = LED_75
Y	y_1 = HL_OFF	y_1 = LED_0	y_1 = LED_100	y_1 = LED_50	y_1 = LED_50	y_1 = LED_75
Y_{act}	y_1 = HL_OFF	y_1 = HL_OFF	y_1 = HL_OFF	y_1 = HL_OFF	y_1 = HL_OFF	y_1 = HL_OFF
L	$l_1(u_1, y_1) = 500\,\mu s$					
Δ_L	$j_{L1}(l_1) \leq 100\,\mu s$					
L_{act}	$l_1(u_1, y_1) = 518\,\mu s$ to $518\,\mu s$, MED $= 518\,\mu s$, AVG $= 518\,\mu s$					
R	$r_1(y_1) = 5000\,\mu s$					
Δ_R	$j_{R1}(r_1) \leq 10\,\mu s$					
R_{act}	$r_1(y_1) = 4998\,\mu s$ to $5002\,\mu s$, MED $= 5000\,\mu s$, AVG $= 5000\,\mu s$					

- Functional requirements cannot be fulfilled
- Expected values are not located at the output
- Non-functional timing requirement are fulfilled
- Latency of the acknowledgement lay within the allowed range

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Conclusion

- Residual bus simulator is directly connected with the SUT
- Message classes and a synchronization procedure are supported
- Non-functional timing requirements are modeled within UML-MARTE
- Abstract test case model models functional and non-functional test data
- Utilization of abstract test cases as simulation model
- Successful utilization for the validation of an RT Ethernet application

Outlook

- Investigate how AUTOSAR and EAST-ADL could co-exist with our approach
- Implement a RBS with a more suitable architecture without dual-port memory
- Analyze the real-time and performance aspects of the new architecture

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